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REALIZATION OF NEGATIVE-IMMITTANCE CONVERTERS AND NEGATIVE RESISTANCES WITH CONTROLLED SOURCES

A THESIS

Presented to

The Faculty of the Graduate Division

by

Chang-Kiang Kuo

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REALIZATION OF NEGATIVE-IMMITTANCE CONVERTERS AND

NEGATIVE RESISTANCES WITH CONTROLLED SOURCES

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SUMMARY

In this research the criteria under which some two-port networks can be compensated with passive networks to behave as ideal NICs have been mathematically derived. These criteria enable us to define the term "nonideal NIC" more realistically. Passive networks required to compensate a nonideal NIC have also been analytically obtained.

Realization of NICs is accomplished by the realization of nonideal NICs first and then compensating them to become ideal ones. A nonideal NIC is obtained by interconnecting two elementary networks, each of which contains a controlled source. A complete list of three-terminal elementary networks each containing a voltage-controlled source and another list of three-terminal elementary networks each containing a current-controlled source have been given with their mathematical matrices. Field-effect transistors and junction transistors are used to realize these controlled sources and to obtain practical elementary networks. A proof is given that indicates that only series-parallel and parallel-series interconnections of two such elementary networks can lead to NIC circuits.

A general discussion is given on the process of realizing an ac model and a dc model NIC from a basic nonideal NIC. An example is presented and its details are discussed.

The stability problem of the NIC is analyzed in this research with two new approaches. It is proved that an NIC is open-circuit unstable and short-circuit stable at one port and short-circuit unstable and open-circuit stable at the other port. A rule to determine the stability

condition at a port has also been established.

Complete lists of basic negative resistance circuits derived from basic nonideal NICs are given. Several typical practical circuits have been investigated.

CHAPTER I

INTRODUCTION

The negative-immittance converter (NIC) is a two-port device that converts an immittance to its own negative within a constant ratio. A negative resistance or a negative capacitance can be obtained by simply connecting a resistor or a capacitor across the output terminals of the device. When expressed in mathematical form, the NIC has a hybrid h matrix of

$$[h] = \begin{bmatrix} 0 & \pm h_{12} \\ \pm h_{21} & 0 \end{bmatrix}$$

where h_{12} and h_{21} are any positive real numbers. If the parameters h_{12} and h_{21} are both positive, the NIC is classified as a current-inversion type NIC (INIC), because the current at both ports is opposite in direction. On the other hand, if they are both negative, then the NIC is classified as a voltage-inversion type NIC (VNIC), because the voltages at both ports are different in direction.

When the NIC was first developed,[1] it was used to realize a negative-resistance (-R) for applications in amplifiers and oscillators. As the result of the discovery of many solid-state devices and the trend of microminiaturization and total integration of electronic circuits, various techniques of filter design[2] and synthesis[3] have been devised with

varying degrees of success by using active elements. Most of these techniques shun the use of the inductance which is impractical for miniaturization and integration. Numerous procedures have been developed which employ the NIC and the negative-resistance for synthesizing active networks. The NIC and the negative-resistance have become one of the most important building blocks in modern circuit design and active network synthesis.

The realization of the NIC is first reported by Merrill[1] using two vacuum triodes. Linvill[4] used two junction transistors to build a voltage-inversion type NIC. Then, Larky[5] used two junction transistors as a high-gain amplifier to realize a current-inversion NIC. Lundry[6] used a high-gain current amplifier to realize a voltage inversion NIC. Later, Braun,[7] aided by the concepts of oport and suport,[8] proposed some NIC circuits using junction transistors. Of all the NICs reported, none was realized by any systematic analytical approach.

The junction transistor, due to its popularity and its longest history among solid-state active devices, has so far been exclusively used in the realization of the NIC and -R. The field-effect transistor (FET), a relatively new solid-state device, has received only limited investigation concerning its application to active networks, in spite of the fact that the FET has many advantages, such as high input impedance, high power gain, low noise, low power consumption, and being producible in vacuum-deposited thin film form.[11] Only two circuits[9,10] that use FETs to realize -R have been reported. No NIC that uses FETs as active elements is known to exist. One of the main objectives of the research is to realize the NIC and the -R employing FETs, as well as junction

transistors, by a general analytical approach.

A practical NIC always contains parasitic parameters. In terms of hybrid h parameters, these parasitic parameters are h_{11} and h_{22}. Larky,[5] Ghausi,[12] and Huelsman[13] have demonstrated that the parasitic parameters of a practical NIC can be nullified by using passive compensation networks. Although it is known that an NIC containing parasitic parameters is a nonideal NIC, and a nonideal NIC can be idealized by passive compensation networks, so far, the term "nonideal NIC" has not been mathematically defined. A nonideal NIC can be defined as a two-port which can be compensated by passive networks to behave as an ideal NIC. In this research, mathematical analysis will be carried out to establish the criteria under which a two-port can be considered a nonideal NIC. These criteria are extremely important to the realization of the NIC because they serve as guidelines as well as a goal in the realization. The criteria are also very important to the analysis of the NIC stability problem, because they give a basis on which the stability problem can be analyzed.

It has been observed[4] that a practical NIC is short-circuit stable and open-circuit unstable (SCS-OCU) at one port, and open-circuit stable and short-circuit unstable (OCS-SCU) at the other port. Recently Brownlie,[14] Hoskins,[15] and Schwarz[16] offered three separate proofs to justify this stability phenomenon by considering the existence of poles or zeros in the right half of the complex-frequency plane. In carrying out their proofs, each of the authors introduced a prerequisite condition. Brownlie assumed the existence of parasitic parameters in the NIC matrix. Hoskins assumed the existence of a time delay in the NIC circuit. Schwarz assumed that either right-half-plane poles or zeros are introduced during

the conversion process. The introduction of a prerequisite condition in the discussion of the NIC stability problem is necessary because without such an assumption an ideal NIC does not have any transient behavior and the stability problem does not arise. The conditions introduced by these authors in verifying the stability phenomenon are not basically sound. They had only confirmed the long observed phenomenon that a NIC is SCS-OCU at one port and OCS-SCU at the other. The problem of determining which port of the NIC is SCS-OCU and which port is OCS-SCU is still left unsolved. In this research, the stability problem of the nonideal NIC will be treated in general, and the ideal NIC as a special case. By applying the criteria derived in this research for the nonideal NIC, it is possible not only to verify the stability phenomenon of the NIC, but also to determine whether a port is SCS-OCU or OCS-SCU.

A negative resistance can be obtained from an NIC by simply connecting a resistor across the output terminals of the NIC. An NIC can actually yield two negative-resistance circuits, one current-controlled and one voltage-controlled. For applications where only -R is required, it is more practical to realize a -R circuit as a one-port than to realize the -R from an NIC because a practical NIC normally is more complex than a practical -R, even though both have the same basic equivalent circuit. For this reason, all -R circuits are separated from the NICs realized in this research.

CHAPTER II

THE NONIDEAL NIC AND ITS COMPENSATION

A nonideal NIC is a two-port which, when compensated by passive networks, will behave as an ideal NIC. More specifically, a nonideal NIC can be considered as an ideal NIC containing parasitic parameters which can be cancelled out by passive compensation networks. Practical NICs always contain parasitic parameters. In the realization of the ideal NIC, it is most practical to start with the realization of the nonideal NIC and then effect the compensation. In order to realize the nonideal NIC, it is essential to establish a set of criteria under which a two-port can be regarded as a nonideal NIC so that there will be a guideline to follow.

In this research, the criteria and the compensation networks for a nonideal NIC will be obtained by mathematical analysis of a two-port network which contains a general two-port and two unknown compensation networks, of which one is in series with and the other is in parallel with each port of the general two-port. By forcing the compensated two-port network to have the matrix of an ideal NIC, the criteria as well as the necessary compensation networks are established. The compensated two-port network is shown in Figure 1. The general two-port network AA'-BB' in Figure 1 has h parameters h_{11}, h_{12}, h_{21} and h_{22} when port AA' is regarded as port 1. Y_1 and Z_2 are respectively an unknown passive admittance and an unknown passive impedance. Conditions on the h parameters and the immittances Y_1 and Z_2 will be defined after the criteria for the

nonideal NIC and the compensation networks are obtained.

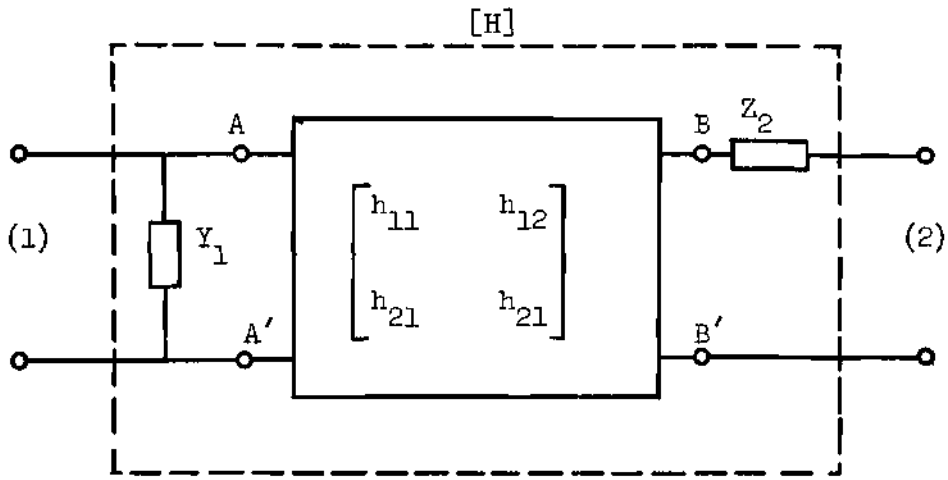


Figure 1. Compensation of a Nonideal NIC.

An ideal NIC is an active two-port which, when terminated in an impedance Z_L at one port, will have an input impedance

$$Z_i = - kZ_L \tag{1}$$

at the other port, where k is an arbitrary positive real number. When a general two-port network having the h parameters h_{11}, h_{12}, h_{21} and h_{22}, is terminated in an impedance Z_L at its port 2, its input impedance at port 1 is

$$Z_i = h_{11} - \frac{h_{12}h_{21}}{h_{22} + 1/Z_L} \tag{2}$$

By comparing Equation (1) with Equation (2), it is clear that the h parameters of an ideal NIC must satisfy the conditions

$$h_{11} = h_{22} = 0 \tag{3}$$

$$h_{12}h_{21} = k \tag{4}$$

It is shown in Appendix I that the matrix [H] of the compensated network in Figure 1 is

$$[H] = \begin{bmatrix} \dfrac{h_{11} + Z_2\Delta h}{1 + h_{11}Y_1 + h_{22}Z_2 + Y_1Z_2\Delta h} & \dfrac{h_{12}}{1 + h_{11}Y_1 + h_{22}Z_2 + Y_1Z_2\Delta h} \\ \dfrac{h_{21}}{1 + h_{11}Y_1 + h_{22}Z_2 + Y_1Z_2\Delta h} & \dfrac{h_{22} + Y_1\Delta h}{1 + h_{11}Y_1 + h_{22}Z_2 + Y_1Z_2\Delta h} \end{bmatrix} \tag{5}$$

where $\Delta h = h_{11}h_{22} - h_{12}h_{21}$. For the compensated network in Figure 1 to behave as an ideal NIC, it is necessary that Equation (3) must first be satisfied, i.e.,

$$Y_1 = -\frac{h_{22}}{\Delta h} \tag{6}$$

and

$$Z_2 = -\frac{h_{11}}{\Delta h} \tag{7}$$

Since both admittance Y_1 and impedance Z_2 are restricted to being passive, both $- h_{22}/\Delta h$ and $- h_{11}/\Delta h$ must be positive-real.

By substituting (6) and (7) into (5), the matrix [H] becomes

$$[H] = \begin{bmatrix} 0 & \frac{\Delta h}{h_{21}} \\ \frac{\Delta h}{h_{12}} & 0 \end{bmatrix} \tag{8}$$

In order to ensure that the compensated network behaves as an ideal NIC, Equation (4) must also be satisfied, or

$$\frac{(\Delta h)^2}{h_{12}h_{21}} = k \tag{9}$$

where k is a positive real number.

The positive-real requirements on immittances (6) and (7), and the relationship (9) are the criteria under which a two-port network can be compensated to become an ideal NIC. These are also the criteria for a two-port network to be a nonideal NIC.

So far, h parameters have been considered as complex numbers. For practical applications, it is important to consider the case where all h parameters are real; because most practical electronic circuits can be considered to have real h parameters at the low-frequency range. These practical electronic circuits are the ones to be used to realize NICs in this research.

When all h parameters of the general two-port network in Figure 1 are real numbers, the compensation networks Y_1 and Z_2 are respectively a positive conductance and a positive resistance and the criteria for the two-port network to be a nonideal NIC can be derived from Equations (6), (7), and (9) as

$$\frac{h_{22}}{\Delta h} \leqq 0 \tag{10}$$

$$\frac{h_{11}}{\Delta h} \leqq 0 \tag{11}$$

$$h_{12}h_{21} > 0 \tag{12}$$

Equation (10) is derived from (6) so that the conductance Y_1 is positive. Equation (11) is derived from (7) so that the resistance Z_2 is positive. Equation (12) is derived from (9) so that the conversion factor k is a positive number. Equations (10) and (11) indicate that both h_{11} and h_{22} must have the same sign or

$$h_{11}h_{22} \geqq 0 \tag{13}$$

and the sign must be opposite to that of Δh.

Conditions (10), (11), and (12) may be satisfied by either of the following two sets of Equations:

$$\text{(I)} \begin{cases} h_{11} \geqq 0,\ h_{22} \geqq 0 & (14) \\ \Delta h < 0 & (15) \\ h_{12}h_{21} > 0 & (16) \end{cases}$$

$$\text{(II)} \begin{cases} h_{11} \leqq 0,\ h_{22} \leqq 0 & (17) \\ \Delta h > 0 & (18) \\ h_{12}h_{21} > 0 & (19) \end{cases}$$

A two-port network that satisfies the conditions listed in set (I) has positive parasitic parameters h_{11} and h_{22} and the product $h_{11}h_{22}$ is less than that of $h_{12}h_{21}$. A two-port network that satisfies the conditions listed in set (II) has negative parasitic parameters h_{11} and h_{22} and the product $h_{11}h_{22}$ is greater than that of $h_{12}h_{21}$. Most practical NICs have the product $h_{11}h_{22}$ less than $h_{12}h_{21}$ and therefore, they fall under the criteria of set (I).

When either h_{11} or h_{22} of the nonideal NIC is zero, only one compensation network is required. For the case $h_{11} = 0$, Equations (6) and (7) become

$$Y_1 = \frac{h_{22}}{h_{12}\ h_{21}} \tag{20}$$

$$Z_2 = 0 \tag{21}$$

and similarly for the case $h_{22} = 0$

$$Y_1 = 0 \tag{22}$$

$$Z_2 = \frac{h_{11}}{h_{12}\, h_{21}} \tag{23}$$

In either case, the matrix [H] of the compensated network is simply (from Equation (8))

$$[H] = \begin{bmatrix} 0 & h_{12} \\ h_{21} & 0 \end{bmatrix} \tag{24}$$

Matrix (24) shows that h_{12}, h_{21} as well as the conversion factor $h_{12}h_{21}$ remain the same after the nonideal NIC has been fully compensated. In the case where both h_{11} and h_{22} are non-zero, the conversion factor will decrease by a factor of $(\Delta h/h_{12}h_{21})^2$ after the nonideal NIC has been compensated. This decrease is indicated from the fact that

$$\frac{(\Delta h)^2}{h_{12}\, h_{21}} \leqq h_{12}h_{21} \tag{25}$$

So far, the criteria for a nonideal NIC have been derived by presupposing that the two-port is oriented as in Figure 1. It is apparent that by turning the compensated NIC network in Figure 1 end over end as shown in Figure 2, the network will still behave as an NIC, and a complementary set of criteria for a nonideal NIC can be derived. Let the h matrix of the two-port AA′-BB′ of Figure 1 be

$$[h] = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \tag{26}$$

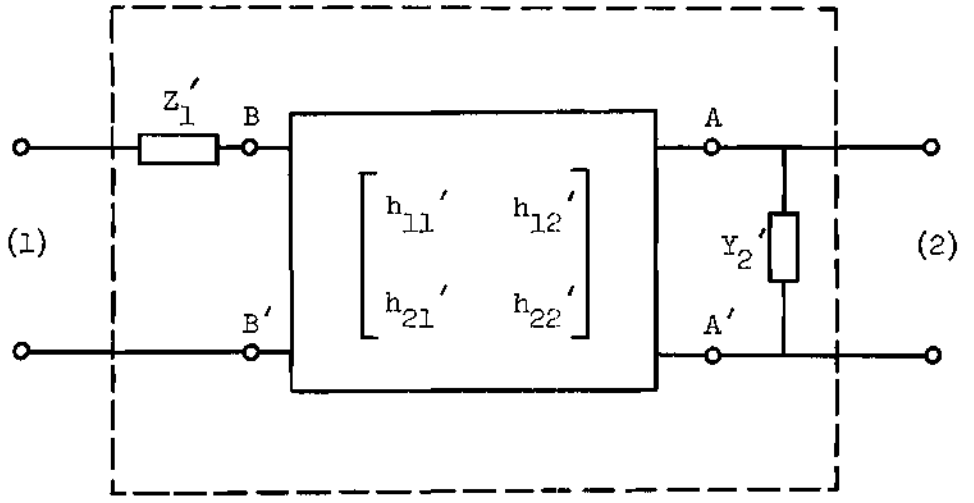


Figure 2. The Complementary Network to the Network in Figure 1.

Then, the h matrix of the two-port BB′-AA′ in Figure 2 is found to be

$$[h'] = \begin{bmatrix} h_{11}' & h_{12}' \\ h_{21}' & h_{22}' \end{bmatrix} = \begin{bmatrix} \frac{h_{11}}{\Delta h} & -\frac{h_{21}}{\Delta h} \\ -\frac{h_{12}}{\Delta h} & \frac{h_{22}}{\Delta h} \end{bmatrix} \tag{27}$$

It is clear that

$$h_{12}' h_{21}' = \frac{h_{12} h_{21}}{(\Delta h)^2} \tag{28}$$

$$\Delta h' \Delta h = 1 \tag{29}$$

From Equations (27), (28), and (29), Equations (6), (7), and (9), can be represented as

$$Y_1 = - h_{22}' \tag{6'}$$

$$Z_2 = - h_{11}' \tag{7'}$$

$$h_{12}' h_{21}' = \frac{1}{k} = k' \tag{9'}$$

where k' is a positive-real number.

The positive-real requirement on (6') and (7') and relationship (9') are the criteria for a two-port network to be a nonideal NIC.

If all of the h parameters are real, the sufficient conditions for a two-port to be compensated to form an ideal NIC are those given by Equations (14) to (19). By substituting these equations into (27), (28), and (29), the following two new sets of equations are obtained for the network of Figure 2 if it is to behave as an NIC.

$$(I')\begin{cases} h_{11}' \geqq 0, \quad h_{22}' \geqq 0 & (30) \\ \Delta h' < 0 & (31) \\ h_{12}' h_{21}' > 0 & (32) \end{cases}$$

$$(II')\begin{cases} h_{11}' \geqq 0, \quad h_{22}' \geqq 0 & (33) \\ \Delta h' > 0 & (34) \\ h_{12}' h_{21}' > 0 & (35) \end{cases}$$

and the compensation immittances are

$$Z_1' = Z_2 = -\frac{h_{11}}{\Delta h} = -h_{11}' \tag{36}$$

$$Y_2' = Y_1 = -\frac{h_{22}}{\Delta h} = -h_{22}' \tag{37}$$

From conditions in sets (I), (I′), (II), and (II′) and Equations (36) and (37), some important respects concerning the nonideal NIC and its compensation can be given as follows:

1. If the h parameters of a two-port satisfy any one of the four sets of conditions (I), (I′), (II), and (II′), then the two-port is a nonideal NIC.

2. If the h parameters of a two-port for one of its orientation satisfy

$$h_{11} \leqq 0, \quad h_{22} \leqq 0, \quad h_{12}h_{21} > 0 \tag{38}$$

then the two-port is a nonideal NIC.

3. The parasitic parameters h_{11} and h_{22} of a nonideal NIC are both negative in at least one orientation, and these parameters can be nulled out by positive immittances of the same magnitudes.

4. A nonideal NIC satisfying conditions (I) and (I′) can be compensated only in one orientation as shown in Figure 1. A nonideal NIC satisfying conditions (II) and (II′) can be compensated in both orientations as in Figure 1 and 2.

CHAPTER III

NONIDEAL CONTROLLED SOURCES AND THE REALIZATION OF THE NIC

Since the NIC is an active two-port network, it can only be realized with active elements. These active elements can be gyrators, negative-immittance inverters (NIV) or controlled sources. For example, the NIC has the transmission matrix [F]

$$[F] = \begin{bmatrix} \mp 1 & 0 \\ 0 & \pm 1 \end{bmatrix} \tag{39}$$

This matrix can be realized by connecting a gyrator and a NIV in series as shown below

$$\begin{bmatrix} \mp 1 & 0 \\ 0 & \pm 1 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} 0 & \pm 1 \\ \mp 1 & 0 \end{bmatrix}$$

NIC Gyrator NIV

$$= \begin{bmatrix} 0 & \mp 1 \\ \pm 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \tag{40}$$

NIV Gyrator

Also, the NIC can be realized by one of the following four circuits, of

which, each contains one ideal controlled source.

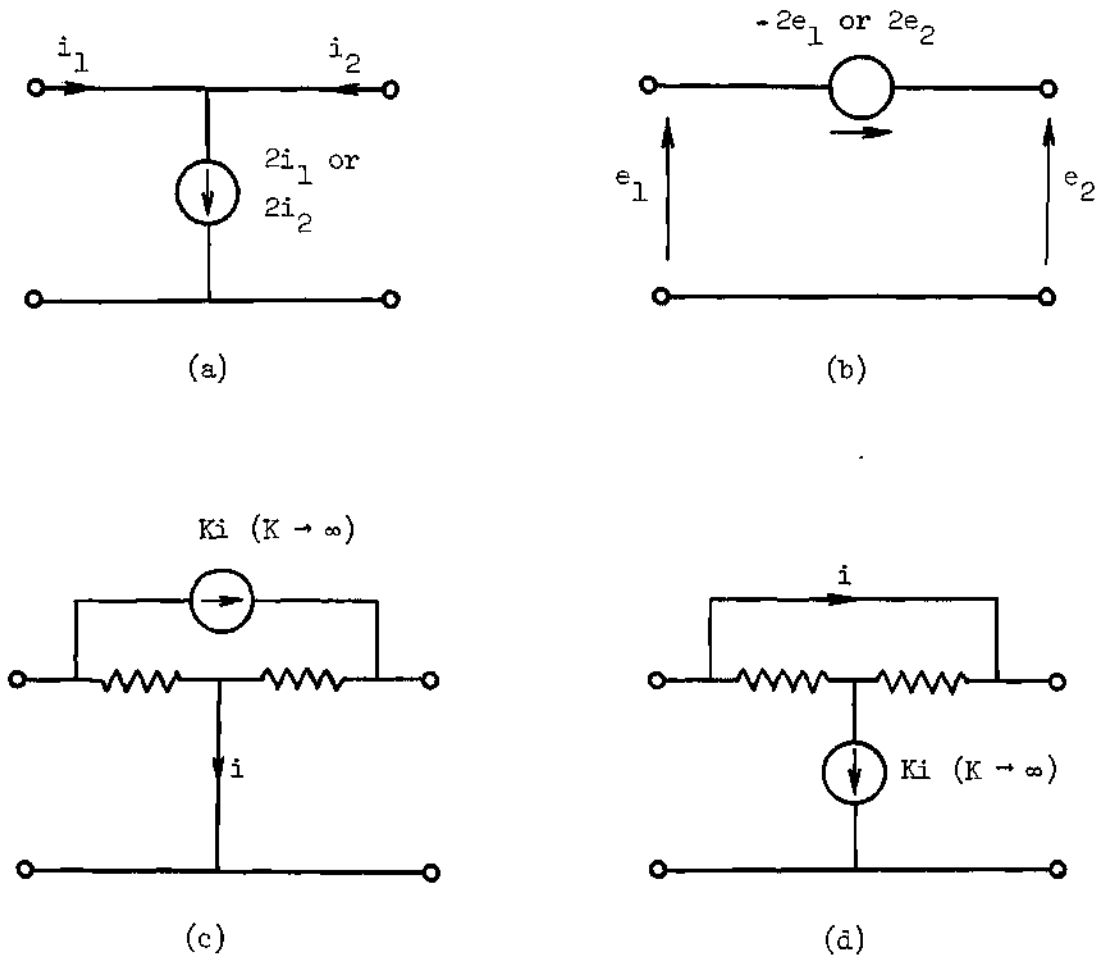


Figure 3. Ideal Controlled Source Realization of NIC.

Realizations of the NIC with a gyrator and a NIV are not desirable because the gyrator and the NIV are usually as complex and difficult to obtain as an NIC. The realizations of the NIC with controlled sources shown in Figure 3 are also unattractive because for practical reasons two amplifiers are required to achieve circuits (a) or (b) and an infinite-gain current-controlled current sources are required to achieve circuits (c) and (d). Nevertheless, some success has been accomplished[17] by using

two transistors to approximate circuits of types (c) and (d) in Figure 3.

It would be desirable to realize the NIC with a minimum number of nonideal controlled sources. The nonideal controlled source here can be represented by a practical active device such as the transistor, the field-effect transistor, the vacuum tube, or integrated-circuit amplifiers. The minimum number of practical controlled sources required to realize an NIC is two. This minimum number can be seen from the facts that an NIC has a positive feedback circuit, and that the minimum number of practical controlled sources required to achieve this positive feedback without using any transformer is two. Using two nonideal controlled sources (or two practical active devices) to realize the NIC is one of the main objectives of this research.

As a first step toward realizing the NIC, the realization of a two-port network whose parameters satisfy the criteria for a nonideal NIC will be studied. In order to realize a nonideal NIC matrix with two controlled sources, an NIC circuit is considered as the combination of two interconnected two-port elementary networks, each of which contains one controlled source. The possible interconnections that can be performed on two two-port networks are:

1) series-series configuration (summation of the two constituent impedance matrices)

2) parallel-parallel configuration (summation of the two constituent admittance matrices)

3) series-parallel configuration (summation of the two constituent hybrid h parameters)

4) parallel-series configuration (summation of the two constituent hybrid g parameters)

5) cascade connection (multiplication of the two chain matrices)

Of the five possible interconnections, series-series and parallel-parallel configurations are not used because, as proved in Appendix II, these configurations will not lead to a nonideal NIC network. Cascade connection is also disregarded because, after a thorough investigation, the chain parameters of all possible elementary networks are found to be positive, and the multiplication of two of these chain matrices will not lead to an NIC chain matrix.

Therefore, the series-parallel and the parallel-series interconnections of two elementary networks are the only configurations that can possibly yield an NIC circuit. Because of the reversibility of both ports of an NIC, if an NIC circuit can be obtained from series-parallel interconnection of two elementary networks, it can also be realized by the parallel-series interconnection. Therefore, series-parallel and parallel-series interconnection really accomplish the same thing in this case; and it is only necessary to carry out one of the two interconnections. In this research, the series-parallel configuration is selected, and the hybrid h parameters will be used throughout the work.

Generally, to effect a direct addition of two elementary hybrid matrices, an ideal transformer is required in the interconnected network. However, when the elementary networks are three-terminal networks, or two-port networks with a common terminal, an ideal transformer is not necessary, provided the input terminals of one of the two constituent networks are reversed. Figure 4 shows such an interconnection of two elementary networks. The hybrid matrix for the interconnected network when represented in terms of the hybrid parameters h_{ij}' and h_{ij}'' of the two constituent networks is:

$$\begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} = \begin{bmatrix} (h_{11}' + h_{11}'') & (h_{12}' - h_{12}'') \\ (h_{21}' - h_{21}'') & (h_{22}' + h_{22}'') \end{bmatrix} \tag{40}$$

Equation (40) indicates that the effect on the h parameters of a two-port network, when the input terminals are interchanged, is to change the signs of both h_{12} and h_{21}. Therefore, when two elementary networks are interconnected as in Figure 4 the h parameters h_{11} and h_{22} for the interconnected network are simply the sum of the two respective constituent parameters and h_{12} and h_{21} are the difference of the two respective constituent parameters. It is of interest to note that if h_{12} and h_{21} of such an interconnected network are both positive (negative), then by the interchange of the position of the two networks, h_{12} and h_{21} will become both negative (positive). This means that a NIC obtained in this research will perform as both INIC and VNIC, depending on which of the two elementary networks has its input terminals reversed.

Elementary Networks

The elementary networks used are each a three-terminal network and must contain a nonideal controlled source. There is an enormous number of three-terminal networks each of which contain one nonideal controlled source and resistors. Since the parameters h_{11} and h_{22} are considered parasitic in the NIC as well as in the elementary networks, the network can be simplified by leaving out those resistors which contribute only to the parameters h_{11} and h_{22}. Hence, the basic configuration of an elementary network is a three-branch network with a common node. Two of the branches contain a resistor each and the third has a controlled

voltage source in series with a resistor.

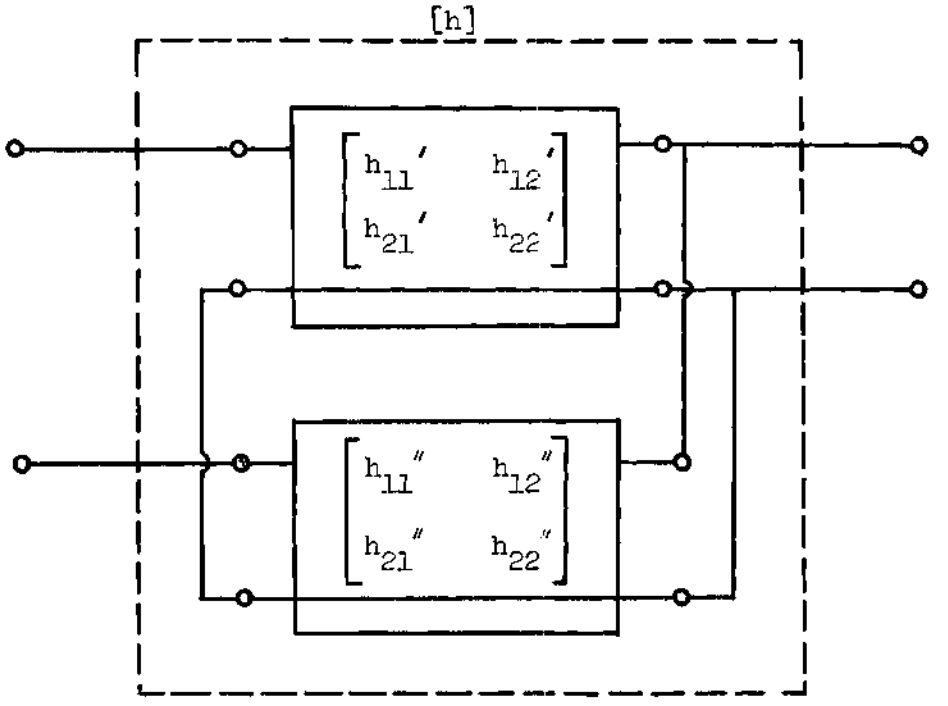


Figure 4. Transformerless Series-Parallel Interconnection of Two Elementary Networks.

There are four types of nonideal controlled sources. They are voltage-controlled current source, voltage-controlled voltage source, current-controlled current source, and current-controlled voltage source. By applying Thevenin's theorem, these four types of nonideal controlled sources can be grouped into only two types --- the voltage-controlled voltage source and the current-controlled voltage source. Figures 5 and 6 show these types of controlled sources. In Figure 5, the parameters g_m and g_d are conductances; and g_m/g_d is the voltage amplification ratio. In Figure 6, the parameters g_o and β are respectively the conductance and the current amplification factor; and β/g_o is the transfer resistance.

The use of these parameters makes it easy to relate them to those of a practical active device. This point will be made clear in the later part of this work.

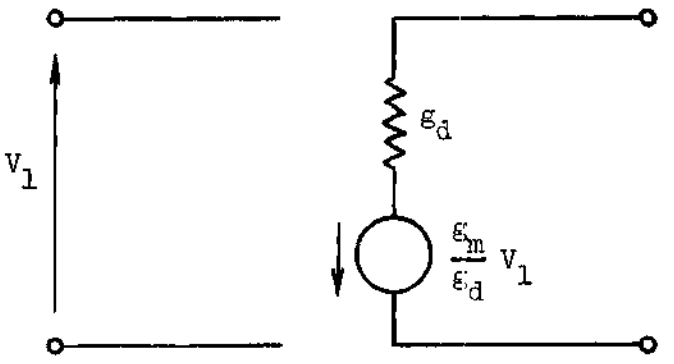


Figure 5. Voltage-Controlled Voltage Source.

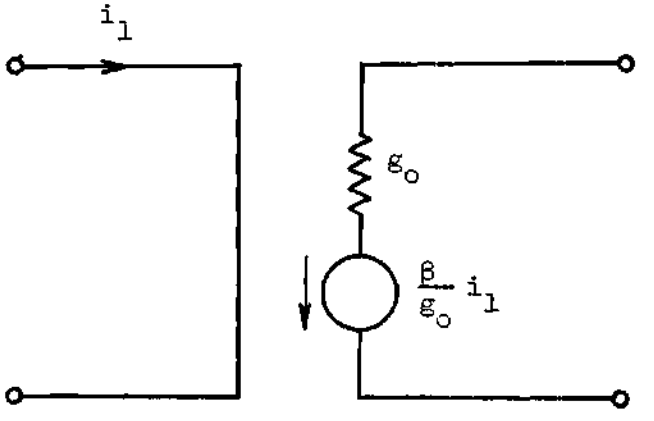


Figure 6. Current-Controlled Voltage Source.

An example of an elementary network which contains a nonideal voltage-controlled voltage source is shown in Figure 7.

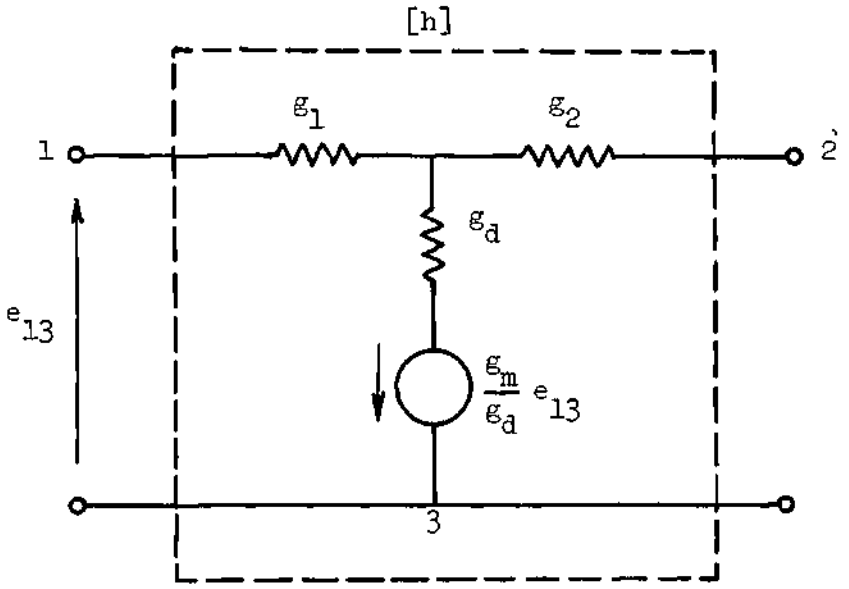


Figure 7. An Elementary Network with a Voltage-Controlled Voltage Source.

The h matrix of the network is given in Equation (41)

$$[h] = \begin{bmatrix} \frac{g_1 + g_2 + g_d}{g_1(g_2 + g_m + g_d)} & \frac{g_2}{(g_2 + g_m + g_d)} \\ \frac{g_2(g_m - g_1)}{g_1(g_2 + g_m + g_d)} & \frac{g_2(g_m + g_d)}{(g_2 + g_m + g_d)} \end{bmatrix} \tag{41}$$

where g_1 and g_2 are both conductances. There are a total of eighteen elementary networks which contain a nonideal voltage-controlled voltage source. They are listed in Appendix III with their respective h matrices.

Practical active devices which can be used to realize a nonideal voltage-controlled voltage source are the triode, the pentode and the

field-effect transistor (FET). In this research the FET (a solid state device) has been chosen because it has a low noise figure, low power consumption and high power gain and can be produced in integrated circuit form. An FET can be either of N-channel type or P-channel type. The difference between these two types is in their dc bias voltages. They are identical in their ac properties. Figures 8 and 9 show the N-channel and P-channel FETs with their respective equivalent circuits where G, D, and S are respectively gate, drain and source, and

$$g_d = \left.\frac{\partial I_D}{\partial V_D}\right|_{V_G} \quad \text{is the output conductance.}$$

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_D} \quad \text{is the transfer conductance.}$$

Because the type of FET to be used in a circuit does not have to be decided until the dc bias of the circuit is being implemented, it is expedient to establish a symbol which represents a general FET of either type. The symbol which is adopted in this thesis is shown in Figure 10.

All elementary networks containing an FET are included in the general nonideal controlled sources listed in Appendix III. After further simplification of all FET equivalent circuits by deleting those resistors that are parasitic, a total of twelve FET elementary networks are found. They are listed in Table 1 with their respective physical circuits and matrices.

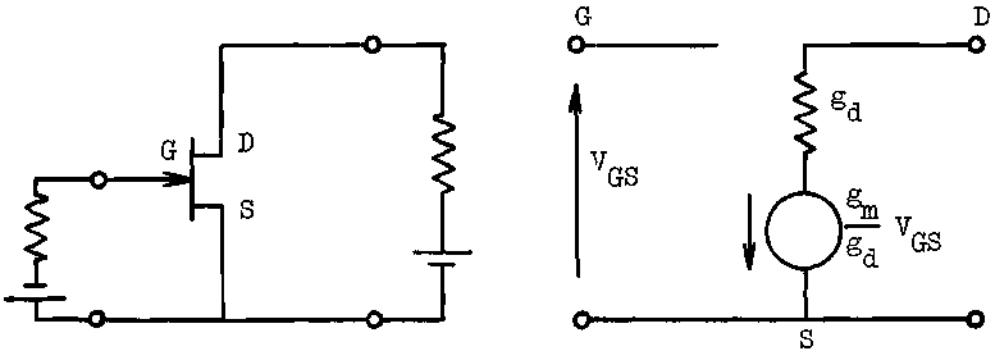


Figure 8. A Biased N-Channel Depletion-Type FET and Its AC Equivalent Circuit.

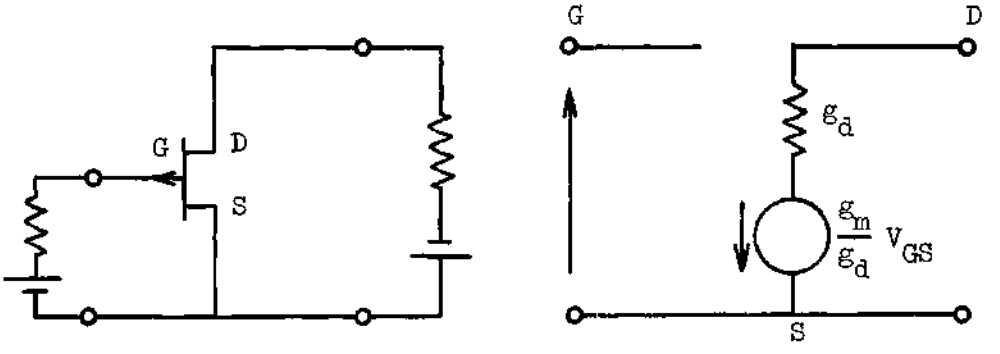


Figure 9. A Biased P-Channel Depletion-Type FET and Its AC Equivalent Circuit.

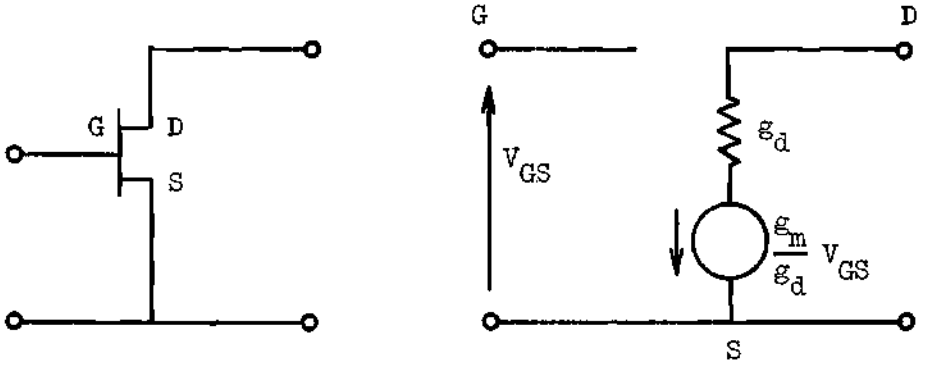
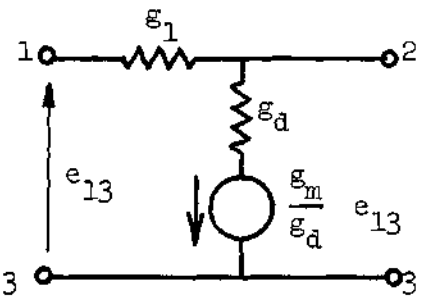
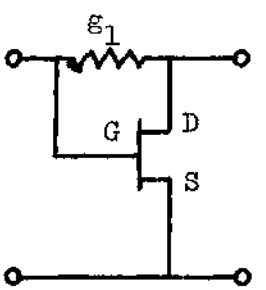
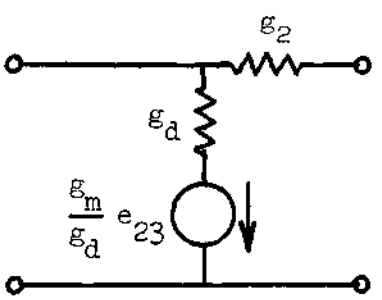
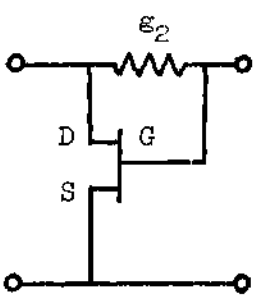
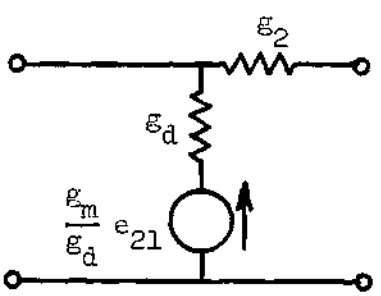
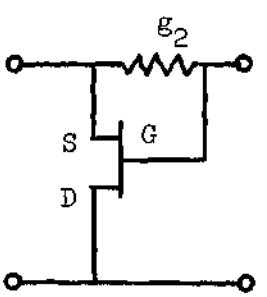
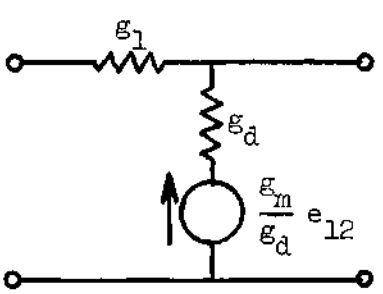
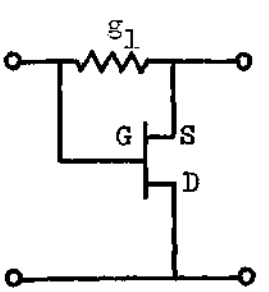
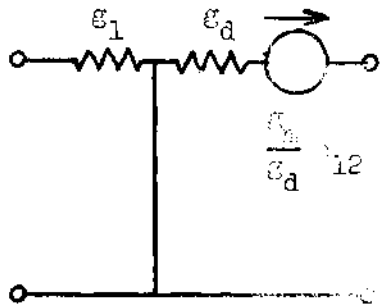


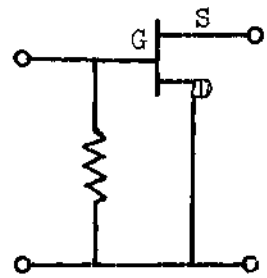
Figure 10. A General FET and Its AC Equivalent Circuit.

Table 1. FET Elementary Networks.

V1			$\begin{bmatrix} \frac{1}{g_1} & 1 \\ \frac{g_m}{g_1} - 1 & g_m + g_d \end{bmatrix}$
V2			$\begin{bmatrix} \frac{1}{g_2+g_d} & \frac{(g_2-g_m)}{g_2+g_g} \\ \frac{-g_2}{g_2+g_d} & \frac{g_2(g_m+g_d)}{g_2+g_d} \end{bmatrix}$
V5			$\begin{bmatrix} \frac{1}{g_2+g_m+g_d} & \frac{g_2+g_m}{g_2+g_m+g_d} \\ \frac{g_2}{g_2+g_m+g_d} & \frac{g_2 g_d}{g_2+g_m+g_d} \end{bmatrix}$
V6			$\begin{bmatrix} \frac{1}{g_1} & 1 \\ -(1+\frac{g_m}{g_1}) & g_d \end{bmatrix}$

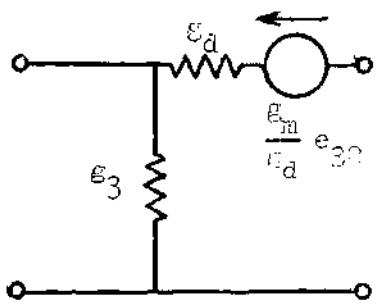
V7

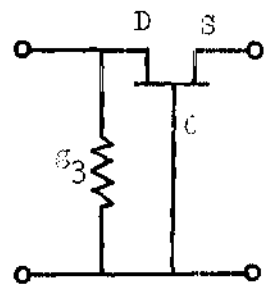




$$\begin{bmatrix} \frac{1}{g_1} & 0 \\ -\frac{g_m}{g_1} & g_m+g_d \end{bmatrix}$$

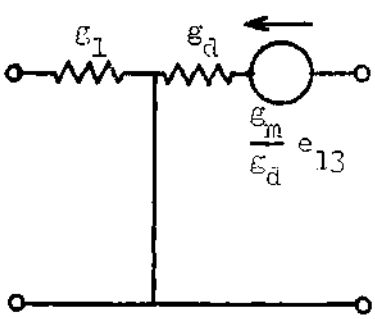
V9

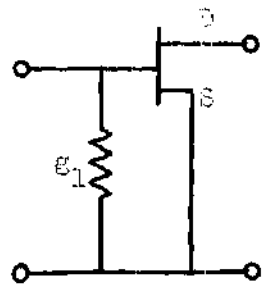




$$\begin{bmatrix} \frac{1}{g_3+g_d} & \frac{g_m+g_d}{g_3+g_d} \\ \frac{-g_d}{g_3+g_d} & \frac{g_3(g_m+g_d)}{g_3+g_d} \end{bmatrix}$$

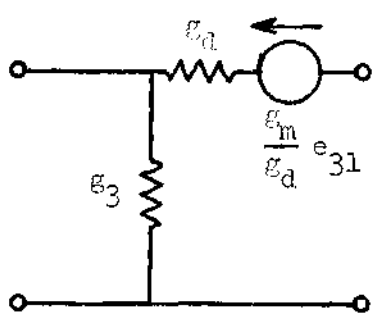
V11

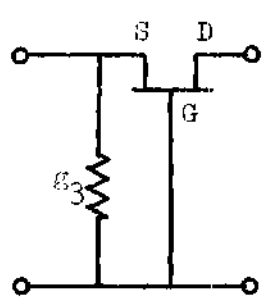




$$\begin{bmatrix} \frac{1}{g_1} & 0 \\ \frac{g_m}{g_1} & g_d \end{bmatrix}$$

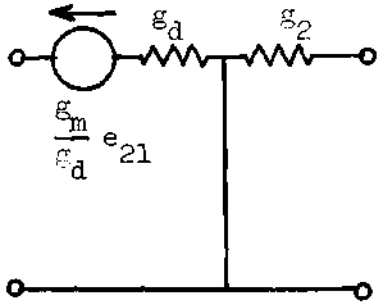
V12

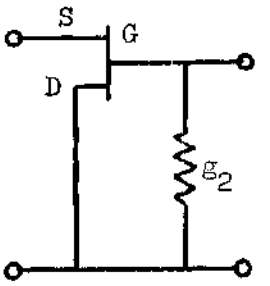




$$\begin{bmatrix} \frac{1}{g_3+g_m+g_d} & \frac{g_d}{g_3+g_m+g_d} \\ \frac{-g_m}{g_3+g_m+g_d} & \frac{g_3 g_d}{g+g_m+g_d} \end{bmatrix}$$

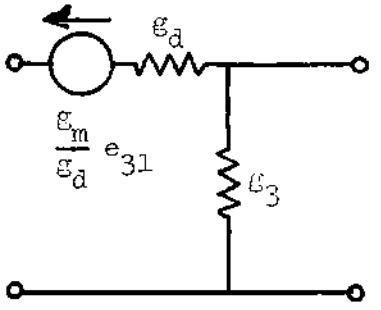
V13

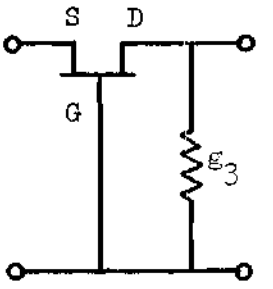




$$\begin{bmatrix} \frac{1}{g_m+g_d} & \frac{g_m}{g_m+g_d} \\ 0 & g_2 \end{bmatrix}$$

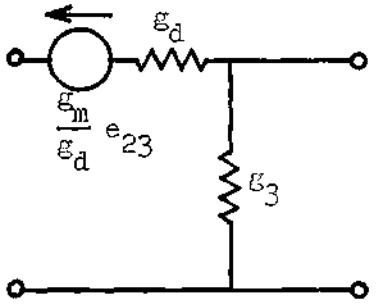
V19

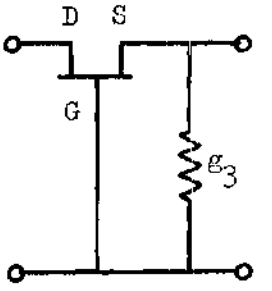




$$\begin{bmatrix} \frac{1}{g_m+g_d} & \frac{g_d}{g_m+g_d} \\ -1 & g_3 \end{bmatrix}$$

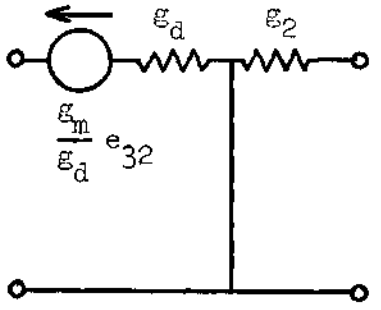
V17

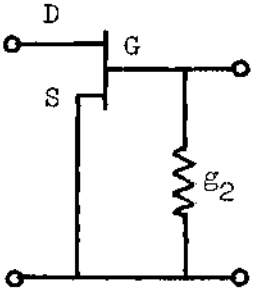




$$\begin{bmatrix} \frac{1}{g_d} & 1 + \frac{g_m}{g_d} \\ -1 & g_3 \end{bmatrix}$$

V18





$$\begin{bmatrix} \frac{1}{g_d} & -\frac{g_m}{g_d} \\ 0 & g_2 \end{bmatrix}$$

This process and technique will now be used to obtain three-terminal networks that contain a nonideal current-controlled voltage source and then to substitute those controlled sources by a practical active device wherever possible. An example of an elementary network which contains a nonideal current-controlled voltage source is shown in Figure 11. The h matrix of the network is shown in Equation (42) where g_1 and g_2 are conductances. The total number of this type of elementary networks is found to be twelve; they are listed in Appendix IV with their respective h matrices.

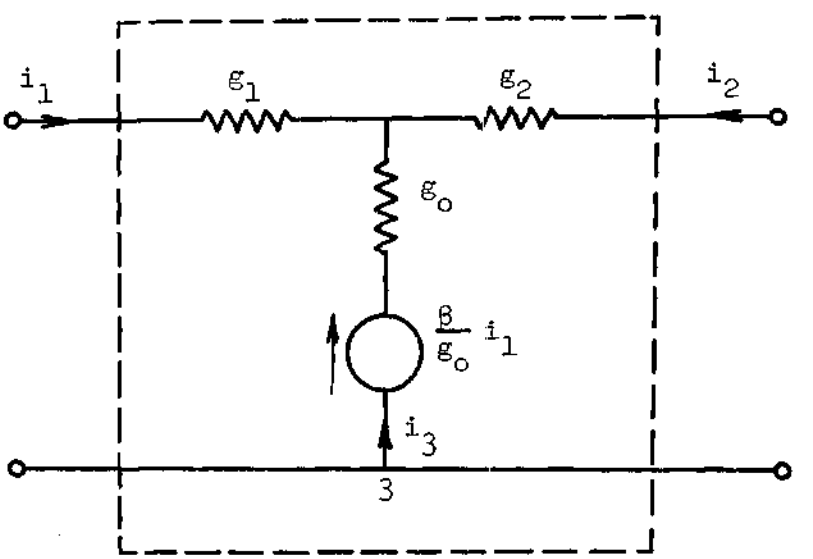


Figure 11. An Elementary Network Containing a Nonideal Current-Controlled Voltage Source.

$$[h] = \begin{bmatrix} \dfrac{g_1 g_o(\beta + 1) + g_2(g_2 + g_o)}{g_1 g_o(g_2 + g_o)} & \dfrac{g_2}{g_2 + g_o} \\ \dfrac{g_2(\beta + 1)}{g_2 + g_o} & \dfrac{g_2 g_o}{g_2 + g_o} \end{bmatrix} \qquad (42)$$

One practical active device which can realize a nonideal current-controlled voltage source is the transistor. There are two types of transistors --- the NPN type and the PNP type. The type of the transistor which will be used in a circuit depends strictly on the dc bias conditions. There is no difference between the two types when considering the ac signal operation. In this research a common symbol has been adopted to represent both types of transistors. The symbol, as well as its ac equivalent circuit, is shown in Figure 12.

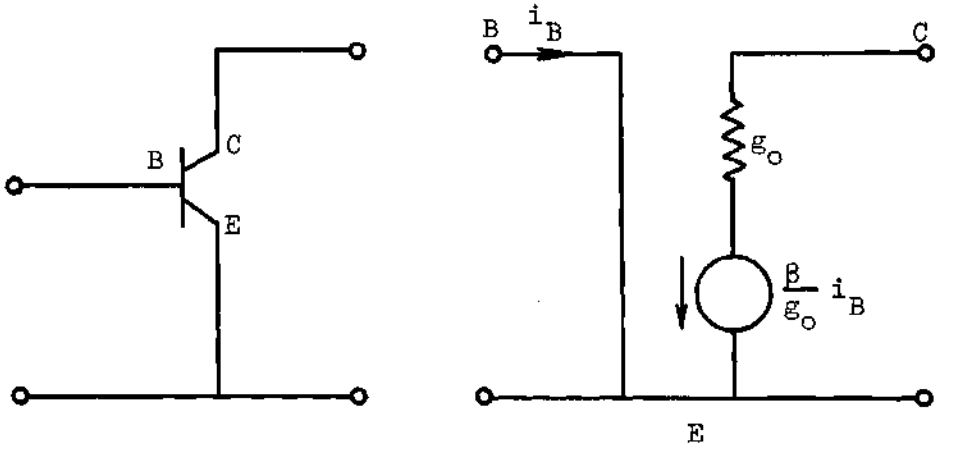
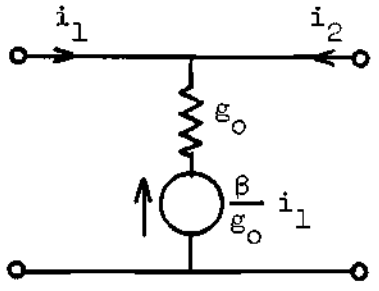


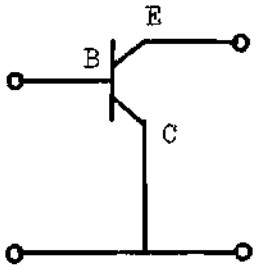
Figure 12. A General Transistor and Its AC Equivalent Circuit.

By substituting a transistor, where possible, into a nonideal current-controlled voltage source of the elementary networks listed in Appendix IV, and after further simplification of all circuits by deleting those resistors which are parasitics, a total of eight transistor elementary circuits are obtained. They are listed in Table 2 with their respective networks and matrices.

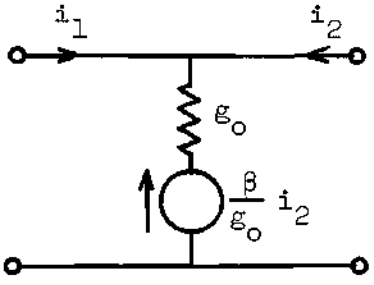
Table 2. Transistor Elementary Networks.



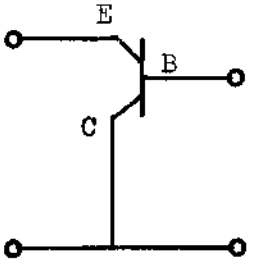
I1



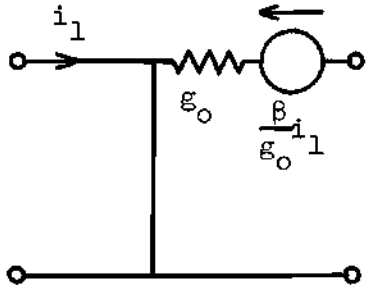
$$\begin{bmatrix} 0 & 1 \\ -(\beta+1) & g_o \end{bmatrix}$$



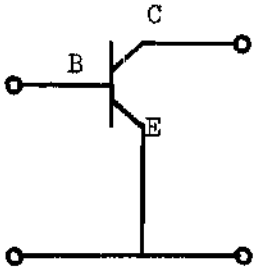
I2



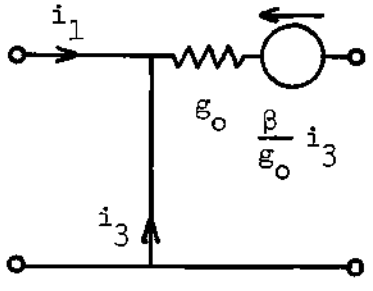
$$\begin{bmatrix} 0 & 1 \\ -\frac{1}{\beta} & g_o \end{bmatrix}$$



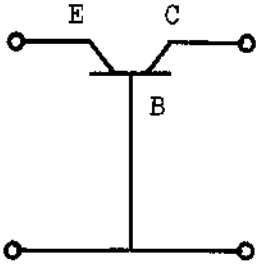
I3



$$\begin{bmatrix} 0 & 0 \\ \beta & g_o \end{bmatrix}$$

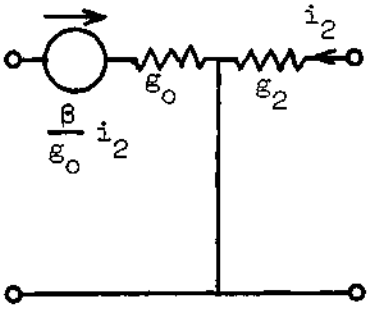


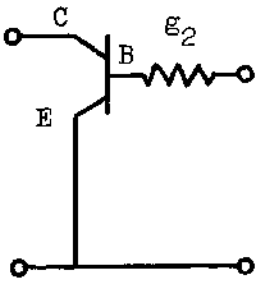
I4



$$\begin{bmatrix} 0 & 0 \\ -\frac{\beta}{\beta+1} & \frac{g_o}{\beta+1} \end{bmatrix}$$

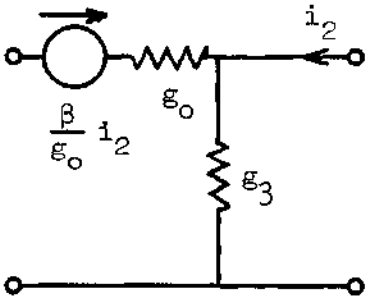
I5

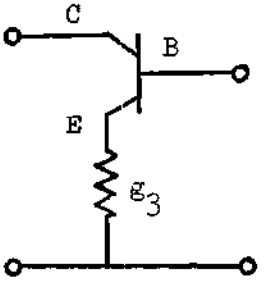




$$\begin{bmatrix} \frac{1}{g_o} & -\frac{\beta g_2}{g_o} \\ 0 & g_2 \end{bmatrix}$$

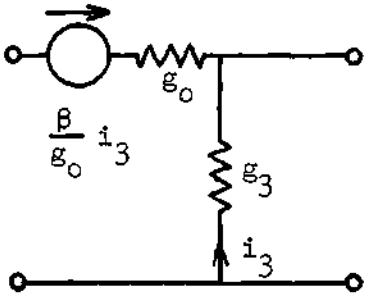
I5′

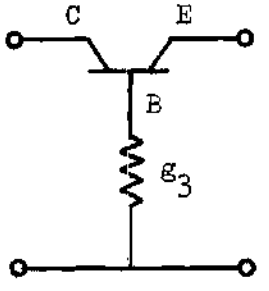




$$\begin{bmatrix} \frac{\beta}{g_o} & \frac{-(\beta g_3 - g_o)}{g_o} \\ -1 & g_3 \end{bmatrix}$$

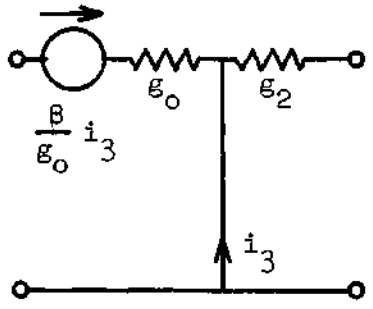
I6

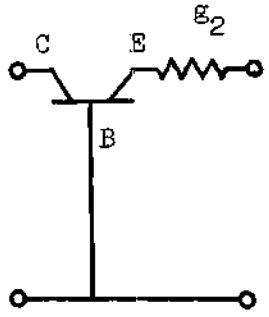




$$\begin{bmatrix} \frac{1}{g_o} & \frac{\beta g_3}{g_o} + 1 \\ -1 & g_3 \end{bmatrix}$$

I6′





$$\begin{bmatrix} \frac{\beta+1}{g_o} & \frac{\beta g_2}{g_o} \\ 0 & g_2 \end{bmatrix}$$

The Realization of the Nonideal NIC

After all practical elementary networks have been found, the nonideal NICs can be obtained by systematically interconnecting the elementary networks two at a time in the manner shown in Figure 4 and using only those interconnected networks whose h parameters satisfy any one of the four sets of conditions (I), (I′), (II), and (II′) in Chapter II. From Tables 1 and 2, the parameters h_{11} and h_{22} of all the elementary networks are positive. Hence, the h parameters of any interconnected networks must satisfy,

$$h_{11} = h_{11}' + h_{11}'' \geq 0 \tag{43}$$

$$h_{22} = h_{22}' + h_{22}'' \geq 0 \tag{44}$$

The only set of conditions that can be satisfied by these two equations is set (I). Therefore, to find out if the interconnected two-port is a nonideal NIC, it is only necessary to check if its parameters satisfy

$$\Delta h < 0 \tag{45}$$

$$h_{12}h_{21} > 0 \tag{46}$$

or

$$(h_{11}' + h_{11}'')(h_{22}' + h_{22}'') - (h_{12}' - h_{12}'')(h_{21}' - h_{21}'') < 0 \tag{47}$$

$$(h_{12}' - h_{12}'')\ (h_{21}' - h_{21}'') > 0 \qquad (48)$$

As mentioned before, a nonideal NIC realized from the series-parallel interconnection of two elementary networks can be either VNIC or INIC depending on which of the constituent networks has its input terminals interchanged. In this research, all basic nonideal NIC circuits will be given in the form of INIC.

The field-effect transistor can be considered as a voltage-controlled current source. Its output conductance g_d is very small, usually in the range of 10^{-5} mhos or less. For simplicity and practicality, the output conductance of the FET will be considered zero.

The basic nonideal NICs obtained from the interconnection of two elementary networks can be separated into three groups according to the types of controlled sources (or active devices) utilized. These three groups are the NICs containing two voltage-controlled sources (or two FETs), the NICs containing two current-controlled sources (or two junction transistors), and the NICs containing one voltage-controlled and one current-controlled sources (or one FET and one transistor). Tables 3, 4, and 5, respectively, list these three groups of nonideal NICs.

Each NIC in these tables has been given an identifier which is the composite of the identifiers of the elementary networks. For example, the identifier I2-V12 indicates not only that the NIC is realized from interconnection of the elementary networks I2 and V12, but also that the elementary network V12 is the one whose input terminals have been reversed. In Tables 3 and 4, all parameters of the first elementary network (I2, for example) have been subscripted as 1, and all parameters of the second

elementary network (V12, for example) have been subscripted as 2 so that the parameters for each active device can be identified.

From NIC circuits and matrices in Tables 3 and 4, it can be found that NICs V1-V2 and V9-V7 are actually the same circuit, and so are NICs V11-V2 and V9-V6, I3-I5 and I5′-I1, and I3-I5′ and I6′-I1.

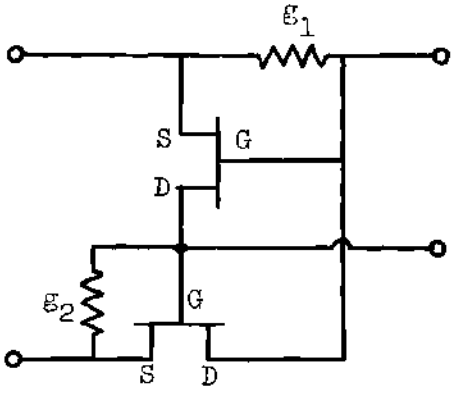
All nonideal NICs listed in Tables 3, 4, and 5 are basic nonideal NIC circuits which conditionally or unconditionally satisfy the criteria for a nonideal NIC. Unconditional nonideal NIC circuits are those whose h_{11} or h_{22} is zero; and $h_{12}h_{21}$ are always positive. They are V5-V12 and I2-I4. Conditional nonideal NIC circuits are those whose h_{11} and h_{22} parameters are nonzero and $h_{12}h_{21}$ are conditionally positive. These circuits include all those listed in Tables 3, 4, and 5, except V5-V12 and I2-I4. For conditional nonideal NIC circuits, care must be taken to satisfy conditions (45) and (46) in implementing these circuits when actual active devices are used.

To develop an operational ideal NIC from a basic nonideal NIC, it is necessary to select the proper types of active devices; to properly bias both active devices; to isolate the circuit from terminated loads which have a tendency to distort the dc bias; and to compensate the parasitic parameters.

Techniques for developing a basic nonideal NIC circuit into an operational ideal NIC are different for different circuits. Although these techniques may be quite similar, there is no single rule that can be followed for all nonideal NIC circuits. Since there are many nonideal NIC circuits found in this research, the development and design details will be carried out for one of the circuits as an example. The circuit selected for this example is V5-V12 which contains two FETs.

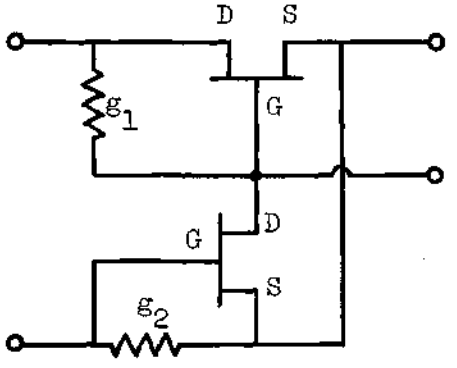
Table 3. Basic FET Nonideal NICs.

V5-V12



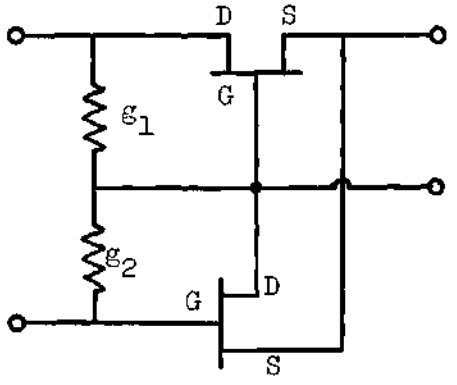
$$\begin{bmatrix} \frac{1}{g_1+g_{m1}} + \frac{1}{g_2+g_{m2}} & 1 \\ \frac{g_{m1}}{g_1+g_{m1}} + \frac{g_2}{g_2+g_{m2}} & 0 \end{bmatrix}$$

V9-V6



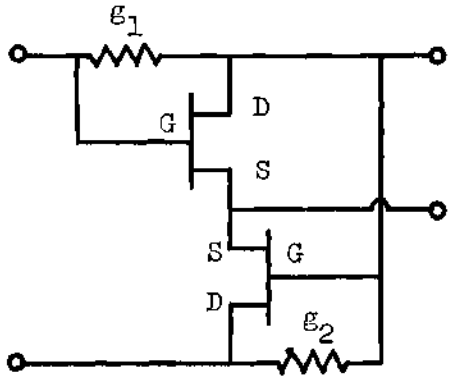
$$\begin{bmatrix} \frac{1}{g_1} + \frac{1}{g_2} & \frac{g_{m1}}{g_1} - 1 \\ 1 + \frac{g_{m2}}{g_2} & g_{m1} \end{bmatrix}$$

V9-V7



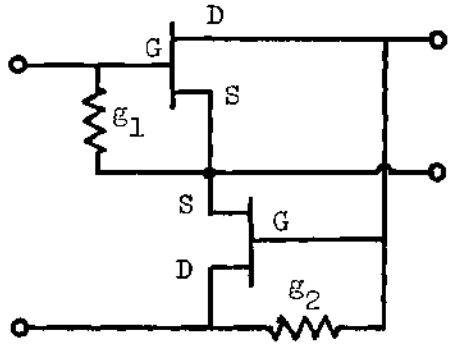
$$\begin{bmatrix} \frac{1}{g_1} + \frac{1}{g_2} & \frac{g_{m1}}{g_1} \\ \frac{g_{m2}}{g_2} & g_{m1} + g_{m2} \end{bmatrix}$$

V1-V2



$$\begin{bmatrix} \frac{1}{g_1} + \frac{1}{g_2} & \frac{g_{m2}}{g_2} \\ \frac{g_{m1}}{g_1} & g_{m1} + g_{m2} \end{bmatrix}$$

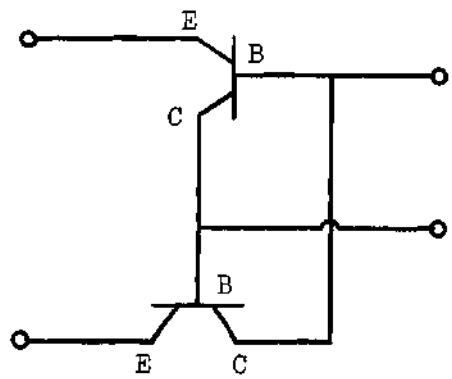
V11-V2



$$\begin{bmatrix} \frac{1}{g_1} + \frac{1}{g_2} & \frac{g_{m2}}{g_2} - 1 \\ \frac{g_{m1}}{g_1} + 1 & g_{m2} \end{bmatrix}$$

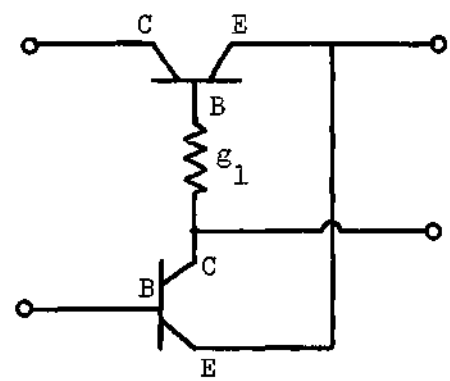
Table 4. Basic Transistor Nonideal NICs.

I2-I4



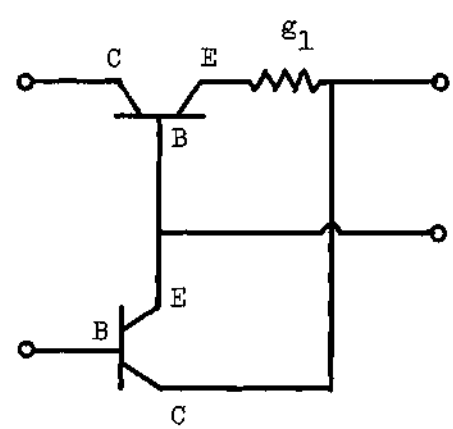
$$\begin{bmatrix} 0 & 1 \\ \frac{\beta_2}{\beta_2+1} - \frac{1}{\beta_1} & g_{o1} + \frac{g_{o2}}{\beta_2+1} \end{bmatrix}$$

I6-I1



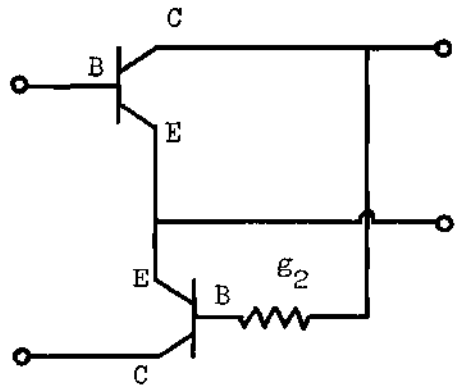
$$\begin{bmatrix} \frac{1}{g_{o1}} & \frac{\beta_1 g_1}{g_{o1}} \\ \beta_2 & g_1 + g_{o2} \end{bmatrix}$$

I6′-I1



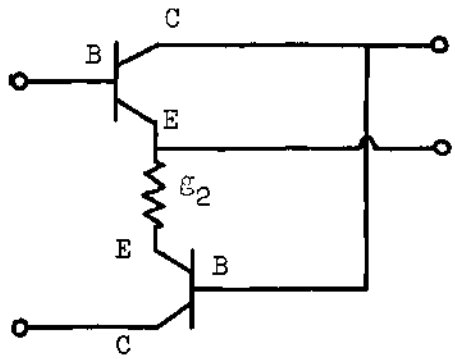
$$\begin{bmatrix} \frac{\beta_1+1}{g_{o1}} & \frac{\beta_1 g_1}{g_{o1}} - 1 \\ \beta_2+1 & g_1 + g_{o2} \end{bmatrix}$$

I3-I5



$$\begin{bmatrix} \frac{1}{g_{o2}} & \frac{\beta_2 g_2}{g_{o2}} \\ \beta_1 & g_2+g_{o1} \end{bmatrix}$$

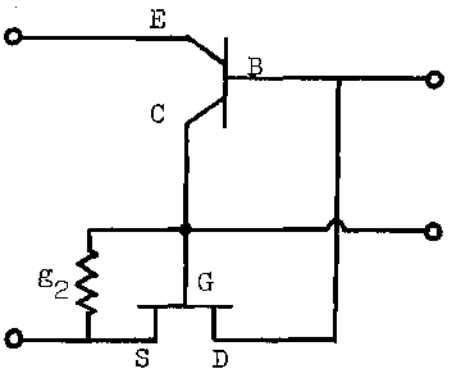
I3-I5′



$$\begin{bmatrix} \frac{\beta_2+1}{g_{o2}} & \frac{\beta_2 g_2}{g_{o2}} - 1 \\ \beta_1+1 & g_2+g_{o1} \end{bmatrix}$$

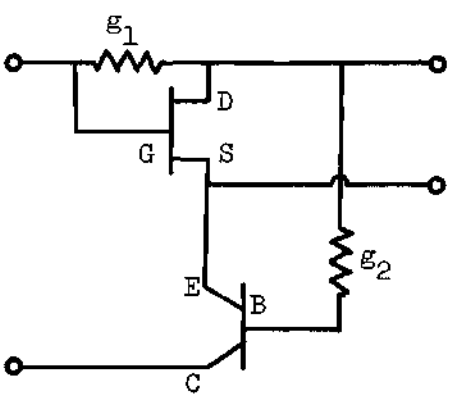
Table 5. Basic Transistor FET Nonideal NICs.

I2-V12



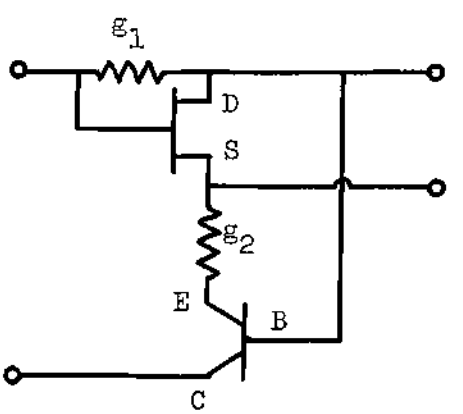
$$\begin{bmatrix} \frac{1}{g_2+g_{m2}} & 1 \\ \frac{g_{m2}}{g_2+g_{m2}} - \frac{1}{\beta} & g_o \end{bmatrix}$$

V1-I5



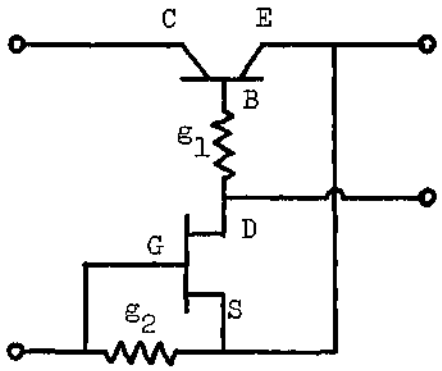
$$\begin{bmatrix} \frac{1}{g_1} + \frac{1}{g_o} & \frac{\beta g_2}{g_o} + 1 \\ \frac{g_m}{g_1} - 1 & g_1 + g_2 \end{bmatrix}$$

V1-I5′



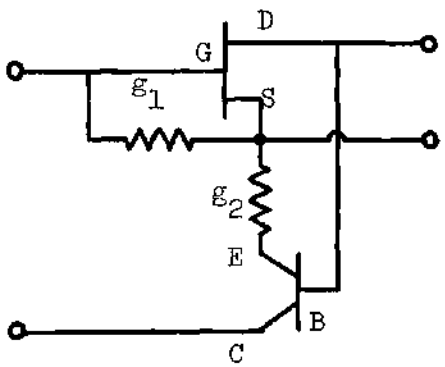
$$\begin{bmatrix} \frac{1}{g_1} + \frac{\beta+1}{g_o} & \frac{\beta g_2}{g_o} \\ \frac{g_m}{g_1} & g_1 + g_2 \end{bmatrix}$$

I6-V1



$$\begin{bmatrix} \frac{1}{g_o} + \frac{1}{g_1} & \frac{\beta g_1}{g_o} \\ \frac{g_m}{g_2} & g_1 \end{bmatrix}$$

V11-I5′



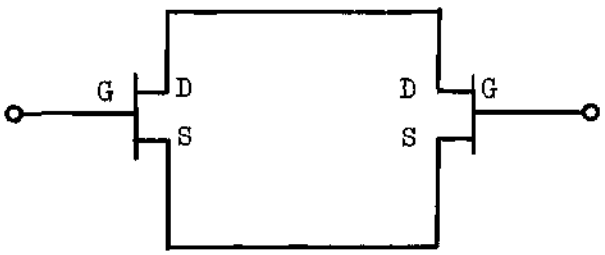
$$\begin{bmatrix} \frac{1}{g_1} + \frac{\beta+1}{g_o} & \frac{\beta g_2}{g_o} \\ \frac{g_m}{g_1} + 1 & g_2 \end{bmatrix} -1$$

DC Bias and AC Model NIC

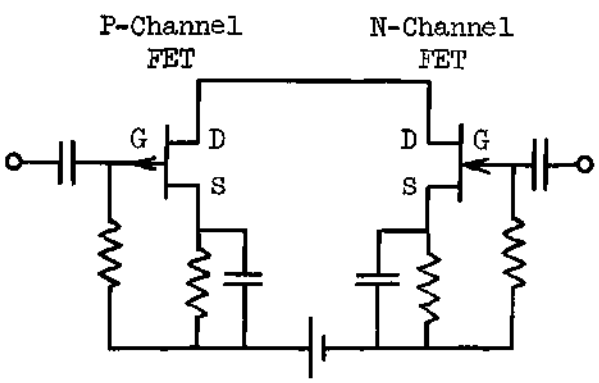
Since the parameters of an active device will properly characterize the active device only when it is operating in a linear active region, it is necessary to bias all active devices so that they operate in this region. Because there are two active devices in an NIC circuit, and because these two active devices must both be properly biased; it is important to select the right types of active devices so that the circuit can be properly biased with the least complexity. The type of active devices which should be used depends on the location and the polarity of the power supply being used. Normally, if all polarities of the power supplies in a circuit are interchanged, the same circuit will still function if all active devices in the circuit are switched to their complementary types.

Normally a bias voltage can be obtained from the voltage drop across a resistor or from using a dc voltage source. When the voltage drop technique is used, a bypass capacitor is required to nullify the effect of the resistor to ac signals. The NIC circuit which contains any bypass capacitor or any blocking capacitor is an ac model, and will not operate down to dc level. An ac-model NIC should be easier to realize than a dc-model because of the freedom in using bypass and blocking capacitors. In this research an ac-model NIC will be realized first.

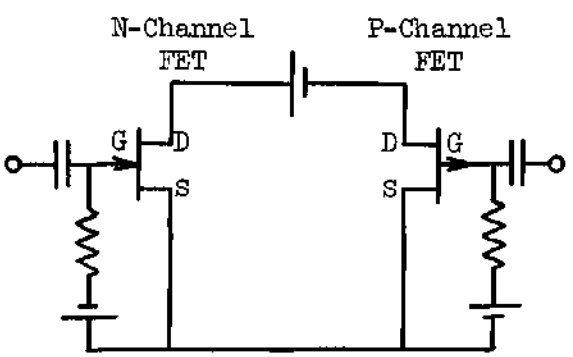
Figure 13 demonstrates how an ac circuit can be biased in different ways with different types of active devices. Circuit (a) in Figure 13 is a basic circuit to be realized. In circuits (b) and (c) the main power supply is in series with the circuit. In circuits (d) and (e) the main power supply is in parallel with the circuit. In circuits (b) and (d), the gate bias voltage is obtained from the voltage drop across a



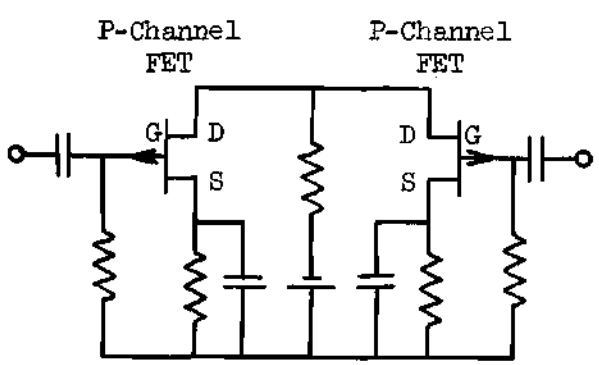
(a)



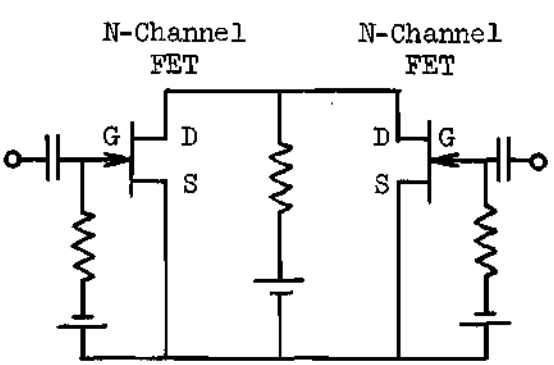
(b)



(c)



(d)



(e)

Figure 13. Example of DC Biasing (Depletion-Type FETs).

resistor; and in circuits (c) and (e), the voltages are supplied from extra voltage sources. In spite of the difference in bias methods, all four biased circuits are equivalent to (a) for ac signals. Of course, there are some advantages and disadvantages for each type of bias. Circuits (b) and (c) require a lower main voltage supply and have less power loss, but they require both active devices to be compatible. In circuits (d) and (e), both active devices can be biased independently, but they need a relatively high main voltage because of the high resistance required in series with the power supply. As to the methods for obtaining the gate bias voltage, circuits (b) and (d) require extra passive components but do not need extra power supplies; circuits (c) and (e) require extra power supplies but fewer passive components. Although two FETs are used in the circuit to illustrate various dc bias methods, the same principle can be applied to other types of circuit that contain different types of active devices.

As mentioned earlier, the two active devices in an NIC circuit must be compatible so that they can both be properly biased. In some circuits it is difficult to fulfill this requirement because of physical limitations on some active devices. These circuits are those listed in Table 4 except I2-I4. The difficulty for these circuits stems from the fact that one terminal of the input port is the collector circuit of a transistor and the other terminal of the same port is the base circuit of another transistor. To bias two transistors, so that one unit's base current is the same as the other unit's collector current, will be extremely difficult.

Example of DC Biasing and an AC Model NIC

The example of NIC circuits to be used for illustrating bias techniques and its ac operations is circuit V5-V12. The basic circuit of the nonideal NIC V5-V12 is shown in Figure 14.

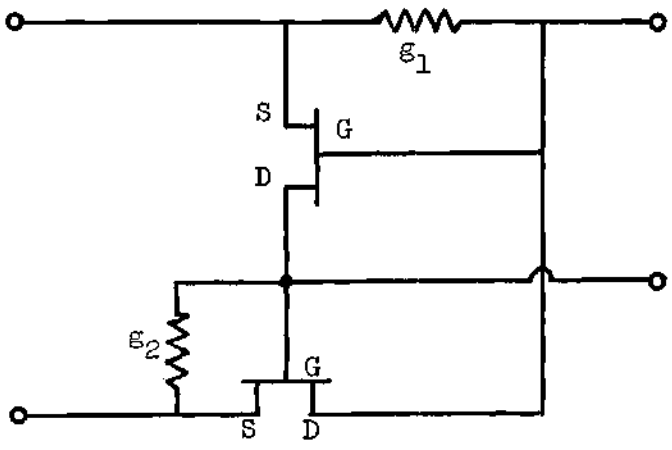


Figure 14. Basic Circuit of V5-V12.

First, the original circuit is redrawn into a more favorable form. This is shown in Figure 15.

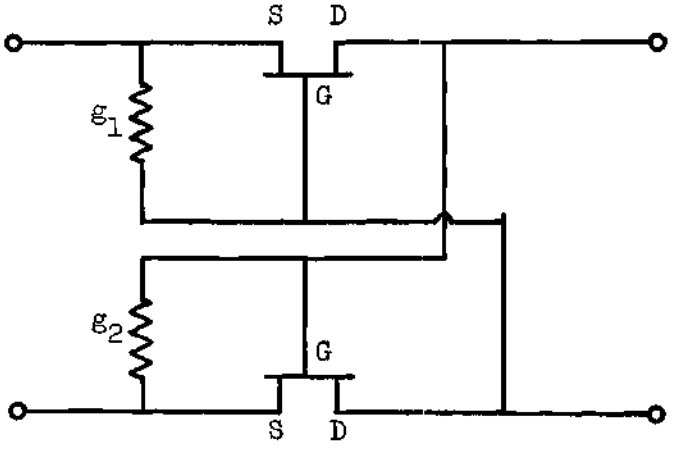


Figure 15. Redrawing of the Circuit in Figure 14.

Conductors g_1 and g_2 are required in the elementary networks to keep the gates of both FET from completely floating. After these two elementary networks are interconnected, both conductors g_1 and g_2 are no longer required, because both gates have been connected to some other parts of the circuit. The circuit in Figure 16 is the basic NIC circuit which will function as an ideal NIC when both FETs are properly biased. Resistors R_9 and R_{10} are compensation immittances.

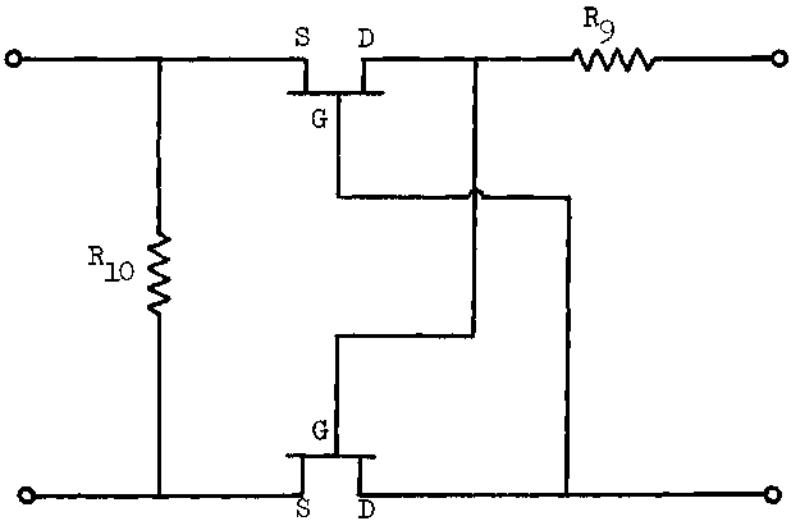


Figure 16. Further Simplified Version of V5-V12.

Because both FETs in the circuit do not form a loop, parallel-type main power supply to both active devices is adopted. Therefore, both FETs must be the same type, either P-channel or N-channel. N-channel FETs were selected because of the availability of these devices. The type of FET used is 2N2608. When the active devices to be used in the NIC circuit have been determined, it is important to locate the optimum operation points for each device from their actual transfer characteristic

curves. The value of bias resistors and supply voltages can then be determined easily with some simple mathematical calculations for any type of bias circuit.

Figure 17 shows the properly biased and compensated ac model NIC of basic circuit V5-V12. The optimum operating point of the FET 2N2608 had been experimentally determined to be I_d = 0.5 ma, V_{GS} = 0.6 volt and V_{SD} = 5 volts. Resistors R_1, R_2, R_3, and R_4 provide the paths for drain and source voltages to both FETs. Ideally, these resistors should be very large, but because a higher main supply voltage is needed for larger resistors, there is a practical limit for the values of these resistors. Source resistor of 22Kn and drain resistor of 10Kn are considered proper, because they will have a total voltage drop of 16 volts. After resistors R_1, R_2, R_3, and R_4 have been selected, the main voltage supply V_1 can be determined as being 21 volts from the equation

$$V_1 = V_{SD} + I_d(R_1 + R_3) \tag{49}$$

Resistors R_7 and R_8 serve as a voltage divider to supply gate voltages to both FETs. The ratio of these two resistors can be determined from the equation

$$V_G = \frac{R_8}{R_7 + R_8} V_1 - I_d R_1 \tag{50}$$

The ratio of R_7/R_8 is found to be 0.81. Therefore, R_7 of 81 Kn and R_8 of 100 Kn are used. Resistors R_5 and R_6 serve to isolate ac signals from dc

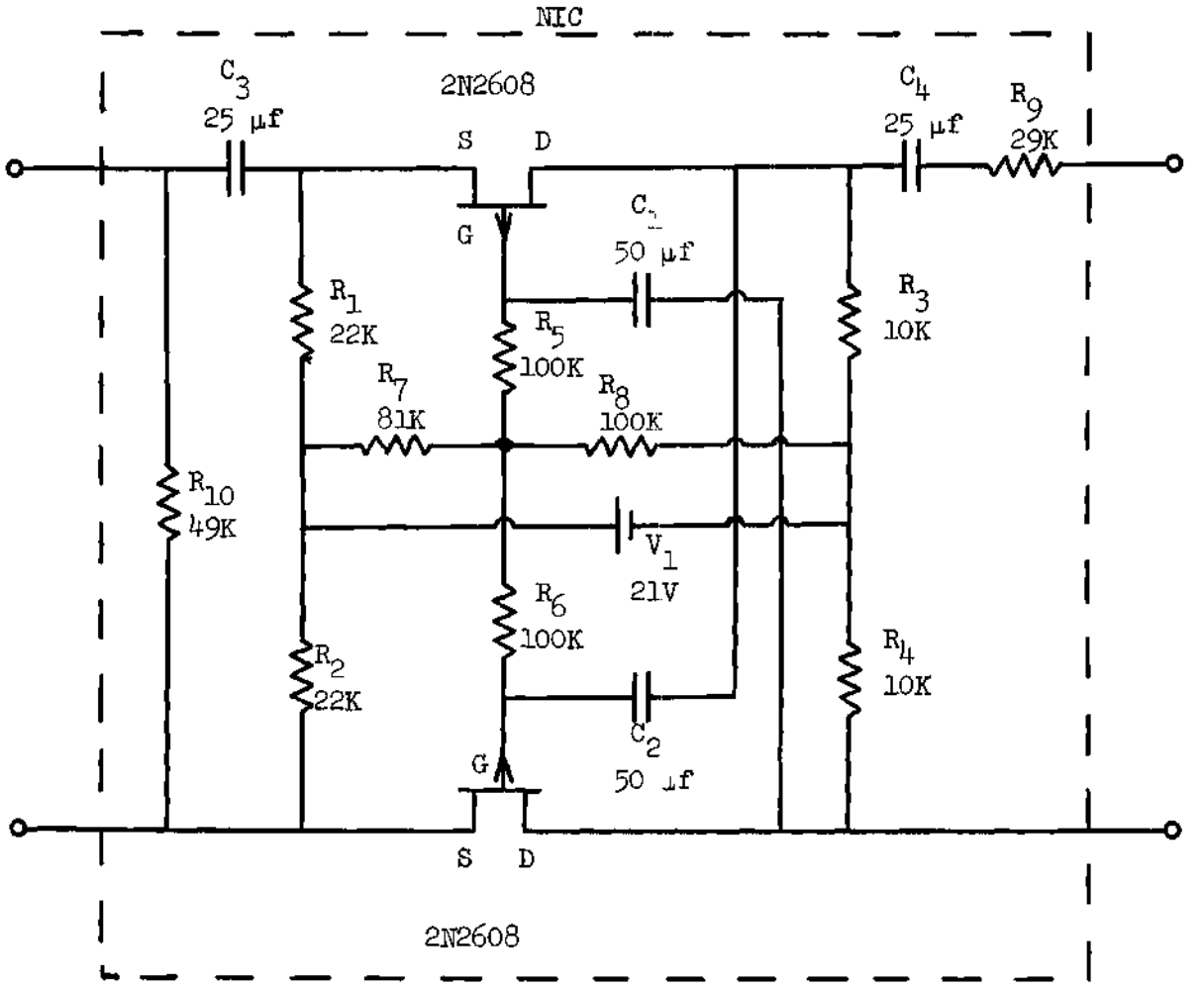


Figure 17. Biased and Compensated NIC V5-V12.

bias circuits. Because the gate leakage current of an FET is extremely small, there is no appreciable voltage drops from these resistors. Any resistors of high resistance can be used.

Capacitors C_1 and C_2 provide short circuits for the ac signals as required in the original circuit of Figure 16. Capacitors C_3 and C_5 are blocking capacitors which isolate the loading networks from distorting the dc bias conditions of both active devices.

Resistors R_9 and R_{10} are compensation networks which can be determined theoretically or experimentally. The theoretical compensation of a nonideal NIC has been thoroughly analyzed in Chapter II. The technique developed there can be followed to obtain compensation networks and the compensated NIC matrix. For the example in this chapter, the matrix of the original nonideal NIC is

$$H = \begin{bmatrix} \frac{1}{g_{m1}} + \frac{1}{g_{m2}} & -1 \\ -1 & 0 \end{bmatrix} \tag{51}$$

When the effect of dc bias circuits is neglected, the compensation networks can be found as

$$R_9 = \left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}\right)$$

$$Y_{10} = 0$$

For the FET 2N2608, the transfer conductance was found to be 800_{μ} mhos, therefore, R_9 should be 25 Kn. The matrix of the compensated network is

$$[H] = \begin{bmatrix} 0 & -1 \\ -1 & 0 \end{bmatrix} \tag{52}$$

Although the exact value of R_9 and R_{10} are easy to determine in theory, they are usually unrealistic because the exact parameters of an active device are difficult to obtain and because the effect of the biasing circuit are rather complicated to ascertain. However, the experimental technique described below achieves the compensation of a practical nonideal ac model NIC rather straightforwardly.

Because the input impedance of an ideal NIC is zero when the opposite port is short-circuited, and is infinite when the opposite port is open-circuited, the compensation resistances R_9 and R_{10} can be obtained separately by using circuit arrangements shown in Figures 18 and 19. These arrangements have taken into consideration the NIC stability problem which will be described in Chapter IV of this thesis. The ac voltage generator and the 100 Kn resistor in Figure 18 simulate an ac current source. The values of R_9 and R_{10} are separately obtained at the null-points of the ac signals shown on the oscilloscope. They are found to be 27 Kn and 49 Kn as indicated in Figure 17.

DC Model NIC

For some applications, a dc-model NIC is more desirable than an ac one as the former will function for very low frequencies and ac

signals. There are more restrictions, however, on a dc model NIC than on an ac one. For an NIC to be a dc model, (1) there must be no bypass or blocking capacitor in the NIC circuit and (2) the circuit must be properly biased under all terminating conditions (range from open to short circuit) at either port. Condition (2) requires that the voltage across a port is zero when the port is open-circuited.

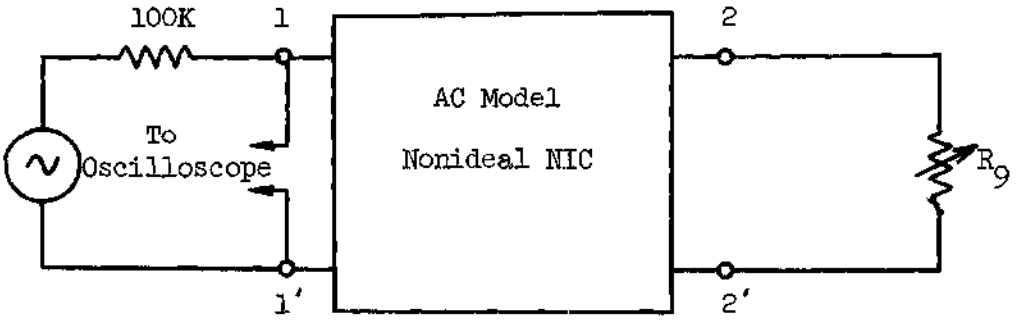


Figure 18. The Circuit Arrangement to Obtain Series Compensation Network.

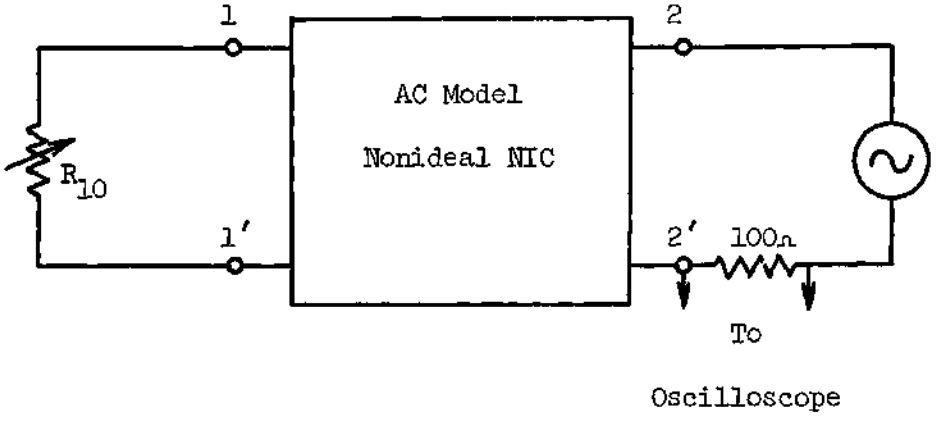


Figure 19. The Circuit Arrangement to Obtain Parallel Compensation Network.

In the realization of a dc model NIC, it is appropriate to start with the ac model NIC circuit which has already been developed. One simple procedure is to replace every capacitor in the circuit by a dc voltage source which has the same magnitude and polarity as those of the capacitor under operating conditions. After a bypass capacitor has been replaced by a voltage source, the resistors used to obtain the bias voltage can be removed. To replace a blocking capacitor at either port of an NIC by a voltage source, it is necessary to consider the capacitor voltage when the port is short-circuited. Figure 20 illustrates the technique of replacing a blocking capacitor by a voltage source. The magnitude of the voltage required to replace a capacitor can be obtained either by theoretical calculation or by experimental measurement. Figure 21 shows the dc model NIC of V5-V12. Note that no voltage source is required to replace the output blocking capacitor in this example.

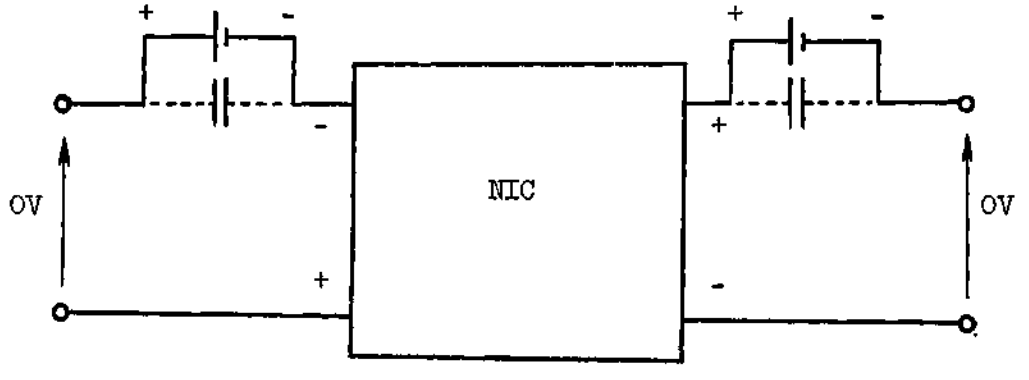


Figure 20. Replacement of a Blocking Capacitor by a Voltage Source.

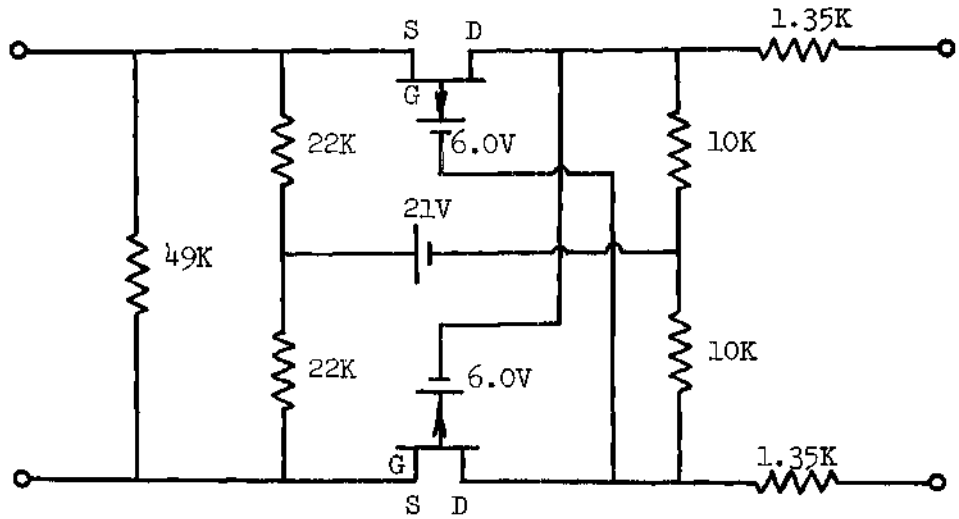


Figure 21. DC Model NIC V5-V12.

The static characteristic of a dc model NIC at either port can be plotted directly on the voltage-current plane as functions of the terminated resistances. The arrangement to plot the v-i characteristic curves depends on whether the port to be investigated is open-circuit stable or short-circuit stable. Figure 22 and 23 show separately the arrangements for plotting the characteristic curves of the OCS and SCS ports.

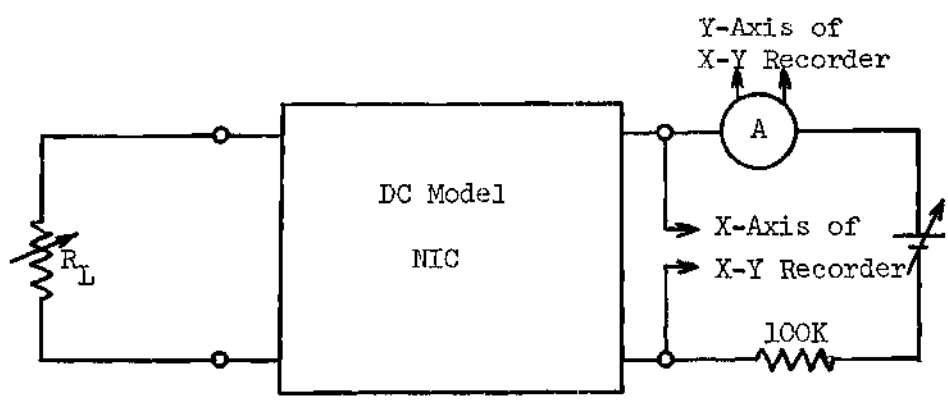


Figure 22. Arrangement to Plot the V-I Characteristic Curves of the OCS Port.

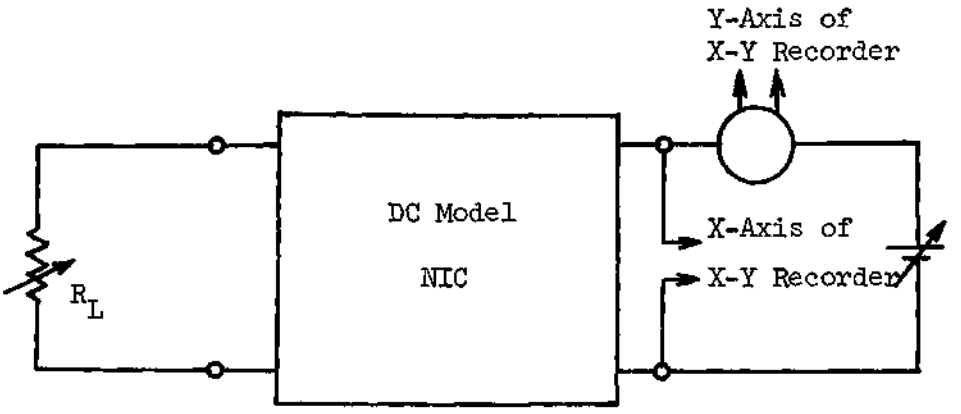


Figure 23. Arrangement to Plot the V-I Characteristic Curves of the SCS Port.

The compensation networks for a dc model NIC can be experimentally obtained by the same arrangements shown in Figures 22 and 23. To find the series compensation resistance, it is only necessary to adjust the resistor R_9 of Figure 22 so that the input resistance is zero or the characteristic curve is vertical on the v-i plane. To find the parallel compensation resistance, it is only necessary to adjust the resistor R_{10} in Figure 23 so that the input resistance is infinite or the characteristic curve is horizontal on the v-i plane. Figures 24 and 25 show respectively the OCS port and SCS port characteristic curves of the dc model NIC V5-V12 shown in Figure 21.

Frequency Response of the NIC

The simplified mathematical models used to represent various active devices in this chapter are accurate only for low frequencies. As the operating frequency becomes higher and higher, capacitances among the

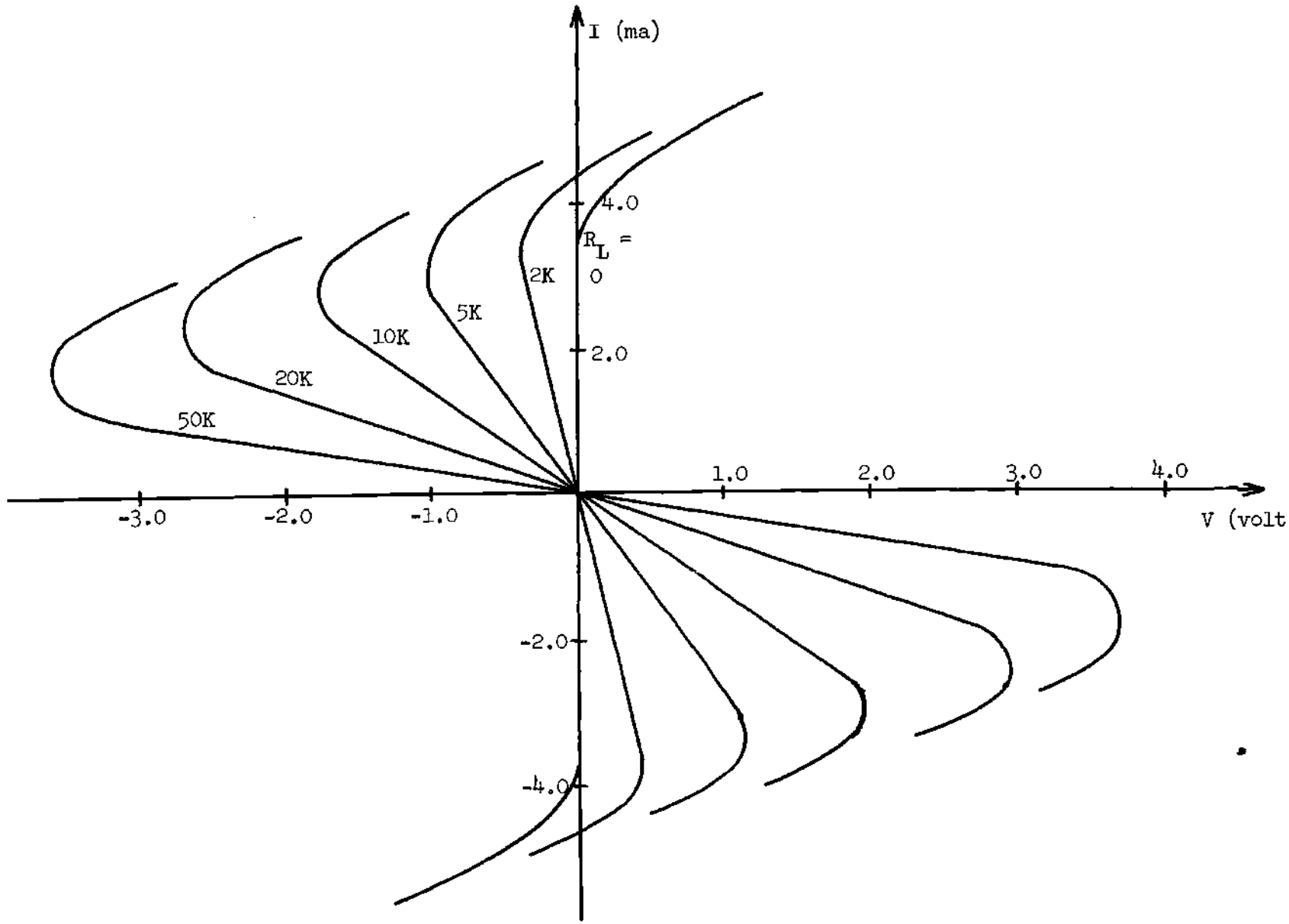


Figure 24. Input Characteristics of DC Model NIC V5-V12 at the OCS Port.

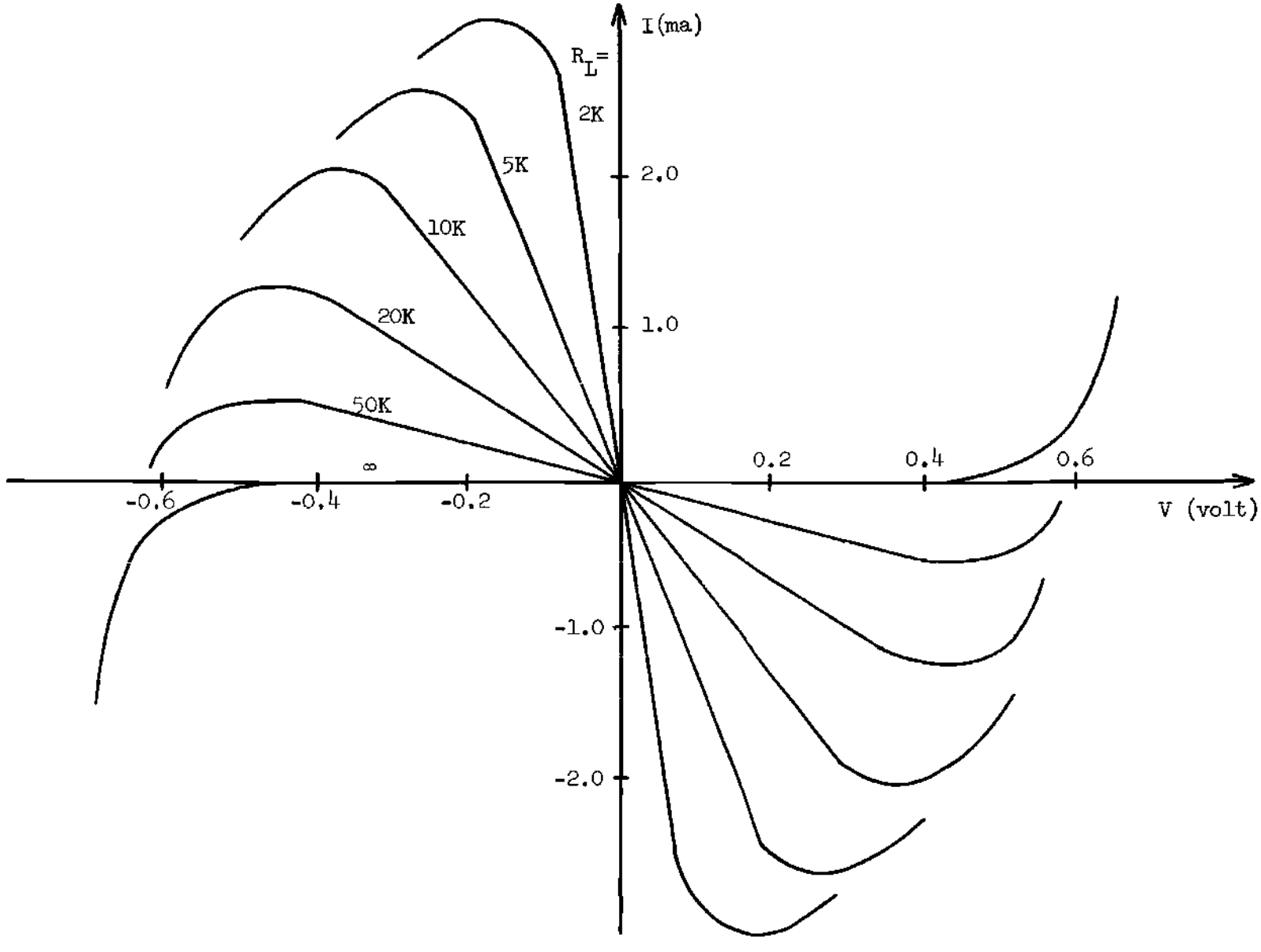


Figure 25. Input Characteristics of DC Model NIC V5-V12 at the SCS Port.

terminals of an active device must be taken into consideration. The simplified equivalent circuits will no longer represent the actual function of those active devices. The transition frequency, at which the simplified equivalent circuit starts to deviate from representing an actual device, depends on the quality and the type of active device used. Normally for an FET, the transition frequency is in the range of several hundred kHz; and for a junction transistor, it is one order or so higher.

The frequency response of a practical NIC depends on the frequency characteristic of the active devices used and the circuit arrangement. The behavior of a practical NIC at high frequencies can be analyzed by using high-frequency model equivalent circuits to represent active devices. A practical equivalent circuit used to represent the FET at high frequency is shown in Figure 26. The equivalent circuit of Figure 26 is modified from the simplified model of Figure 10 by adding capacitor C_{GS} between the gate and the source and capacitor C_{GD} between the gate and the drain. A useful equivalent circuit which will represent the junction transistor at high frequencies is shown in Figure 27.

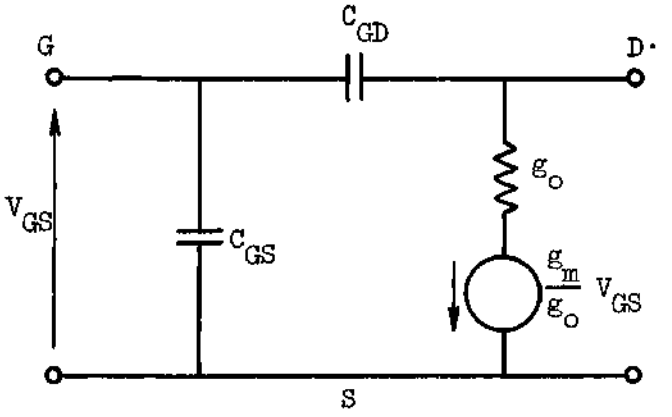


Figure 26. High-Frequency FET Equivalent-Circuit.

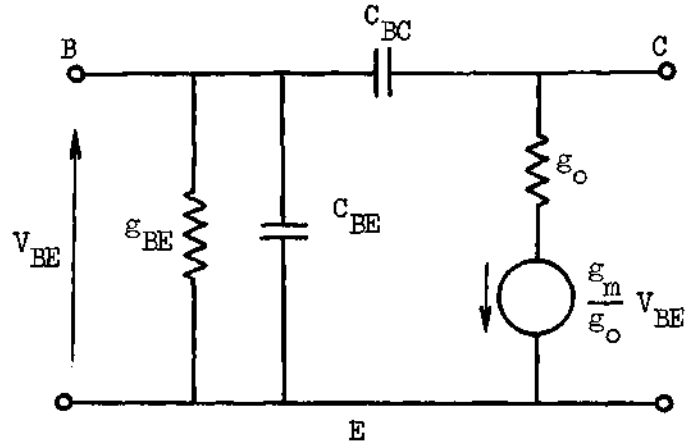


Figure 27. High-Frequency Transistor Equivalent-Circuit.

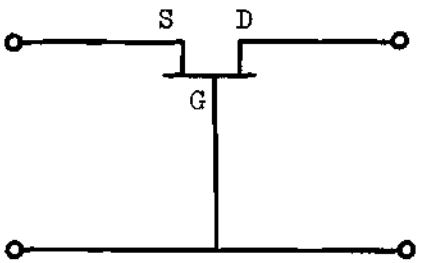
To analyze the NIC containing only transistors, it is more practical to modify the equivalent circuit in Figure 27 such that the frequency effect of the transistor is completely combined into the current amplification β and the simplified equivalent circuit of Figure 12 can be used. The value of β in the high frequency equivalent circuit should be of the form[4]

$$\beta = \beta_o \frac{1}{1 + j \frac{f}{f_o}} \tag{53}$$

where f_o is the β cut-off frequency.

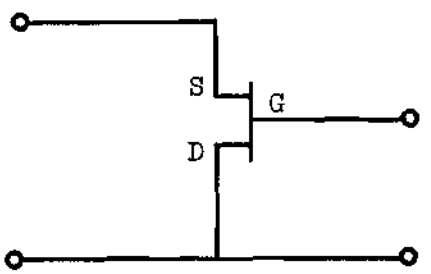
To illustrate the analytical approach for studying the frequency response of an NIC, the NIC V5-V12 will again be used as an example. The FET elementary circuits V5 and V12 and their high frequency matrices are respectively shown in Figures 28 and 29. If the FETs in V5 and V12 are

identical, then the matrix of the NIC V5-V12 can be derived as (54)



$$[H] = \begin{bmatrix} \frac{1}{g_m + sC_{sg}} & 0 \\ \frac{-g_m}{g_m + sC_{sg}} & \frac{sg_mC_{dg}}{g_m + sC_{sg}} \end{bmatrix}$$

Figure 28. Elementary Circuit V5 and Its Matrix.



$$[H] = \begin{bmatrix} \frac{1}{g_m + sC_{sg}} & 1 \\ \frac{sC_{sg}}{g_m + sC_{sg}} & \frac{sg_mC_{dg}}{g_m + sC_{sg}} \end{bmatrix}$$

Figure 29. Elementary Circuit V12 and Its Matrix.

$$[H] = \begin{bmatrix} \frac{2}{g_m + sC_{sg}} & -1 \\ -1 & \frac{2sg_mC_{dg}}{g_m + sC_{sg}} \end{bmatrix} \qquad (54)$$

From matrix (54), the input impedance of the NIC at port 1 can be found from Equation (2) as

$$Z_i = \frac{g_m(2Y_L - g_m) + 2(2g_mC_{dg} - g_mC_{sg} + Y_LC_{sg})s - }{g_m^2Y_L + 2g_m(Y_LC_{sg} + g_mC_{dg})s +}$$

$$\frac{C_{sg}^2s^2}{(Y_LC_{sg}^2 + 2g_mC_{dg}C_{sg})s^2} \qquad (55)$$

When the input impedance of the NIC is represented as in Equation (55), the series compensation network is automatically taken care of by the terminating admittance Y_L. It is not necessary to identify the compensation resistance separately in the equation. In order to plot the input impedance Z_i of Equation (55) as a function of frequency, a digital computer has been employed. The computer program developed is shown in Appendix V and the result of the computer calculation is shown as curve A of Figure 30.

To study the frequency response of the NIC experimentally, the circuit arrangement of Figure 31 was used. Basically, the arrangement is to obtain the input impedance of the NIC as a function of frequency by comparing the amplitude and phase of the voltage at the input of the NIC to those of the input current. The experimental result of this study is shown as curve B of Figure 30.

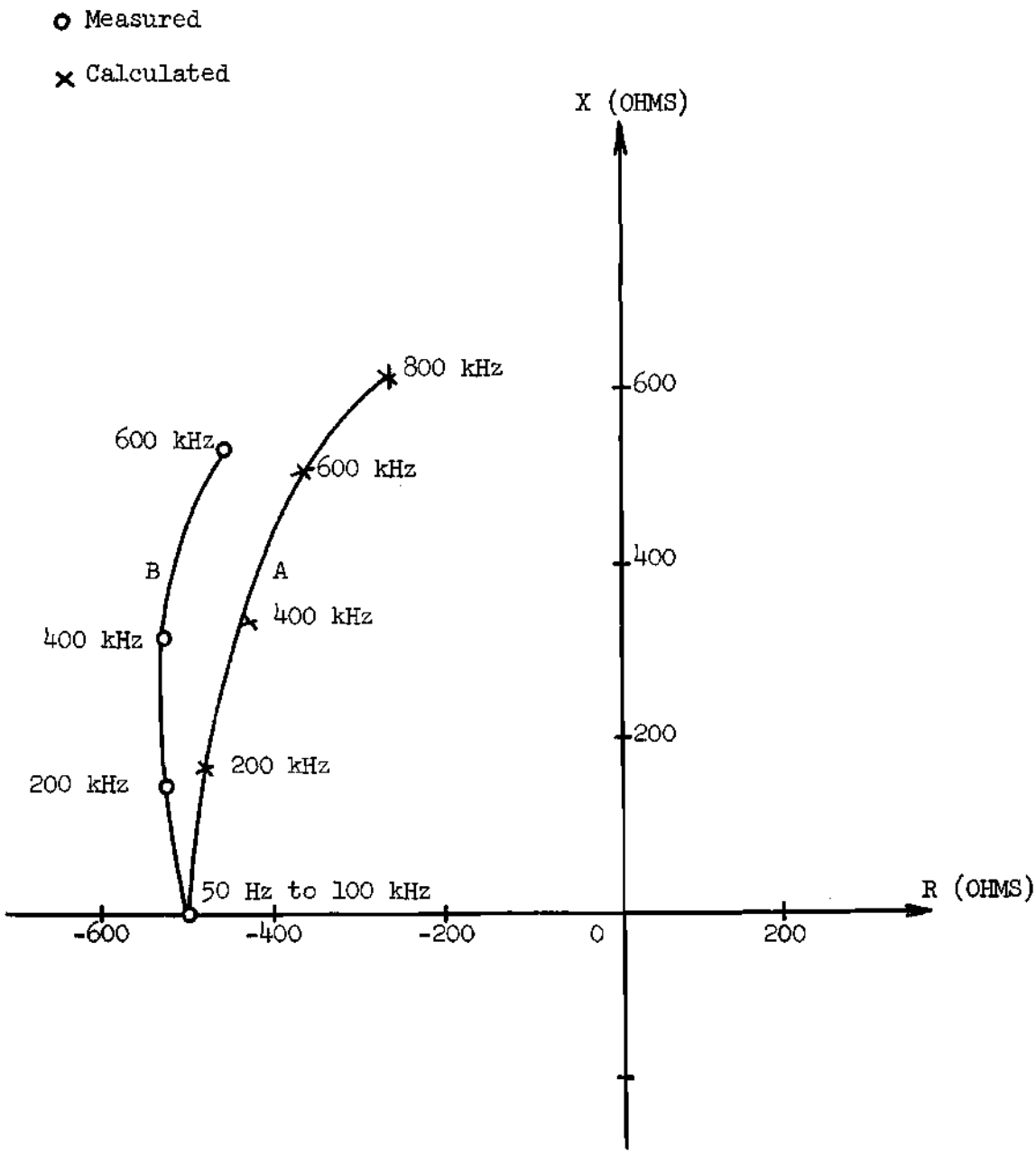


Figure 30. Frequency Response of the NIC V5-V12.

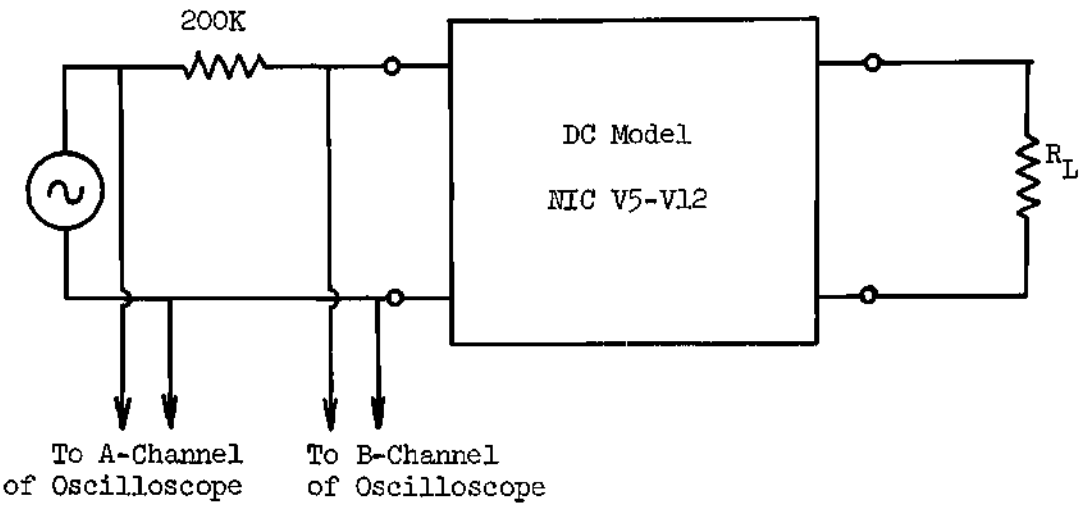


Figure 31. An Arrangement to Study the Frequency Response of the NIC.

CHAPTER IV

THE STABILITY OF THE NIC

Since the NIC converts an immittance into its own negative, a passive immittance terminated at one port of the NIC will give rise to some negative real part of the immittance at the other port. Hence, the NIC is a potentially unstable two-port --- a two-port which when terminated in some passive networks at both ports, can become unstable. Whether an NIC will remain stable or not in a system depends on the properties of networks that are connected to the NIC. To investigate the stability of the NIC, it is necessary to consider the NIC and its terminating networks (or the system) as a whole. It is meaningless to try to analyze the stability problem of the NIC alone. In other words, the study of the stability problem of the NIC is to investigate the effect of loading conditions at both ports on the stability of the NIC itself. This investigation can be made in general terms of whether a port of the NIC is open-circuit unstable (OCU), short-circuit unstable (SCU), short-circuit stable (SCS), or open-circuit stable (OCS). Even if a port of the NIC is determined to be SCS it is not necessary that the NIC be stable only when this port is short-circuited. Rather, the NIC will usually still remain stable if the port is terminated in a small impedance. This argument is also true for the OCS port of an NIC. The NIC will normally still be stable if the port is connected to a large impedance. Above all, the stability of a particular NIC when terminated in some particular passive networks can only be predicted by a complete analysis of the system.

OCS or SCS will serve only as a guideline in terminating an NIC for stable operation.

It has been observed[4] that a practical NIC is always SCS and OCU at one port, and OCS and SCU at the other port. In this research, two different approaches will be employed to prove this stability property of the practical NIC. The first approach is to consider the NIC and its terminating networks as a linear frequency dependent system. To prove that the practical NIC is SCS-OCU at one port, and OCS-SCU at the other port it is necessary to prove that the input impedance at one port has no right-half-plane pole but has right-half-plane zero and that the input admittance at the other port has no right-half-plane pole but has right-half-plane zero. The second approach employed to prove the stability property of the practical NIC is to consider the NIC, when terminated in resistors, as a nonlinear system. To prove that the practical NIC is SCS-OCU at one port and OCS-SCU at the other port it is necessary to prove that the negative input resistance of the NIC is voltage-controlled at one port and current-controlled at the other port. The results derived from both approaches, in determining whether a practical NIC port is SCS-OCU or OCS-SCU should lead to the same conclusion.

The stability problem does not arise in an ideal NIC because the behavior at both ports of the ideal NIC are identical. Only in a practical NIC do we need to be concerned with the stability problem. Therefore, the practical NIC will be used in the investigation of the stability problem. Before we begin to justify the stability problem of the NIC it is necessary to define mathematically the term "practical NIC." Since a practical NIC is not an ideal one, it is logical to identify it with the

nonideal NIC. In Chapter II of this text, the criteria for a two-port to be a nonideal NIC have been given as conditions in sets I-I′ and II-II′ [Equation (30)-(35)]. To define the criteria for a practical NIC it is only necessary to determine if the network parameters satisfy the conditions of sets either I-I′ or II-II′ or both. It can easily be found that the practical NIC is the class of two-port which will satisfy only the conditions of sets I-I′. One of the conditions in sets II-II′ requires parameters h_{11} and h_{22} to be negative in both orientations. This condition can not be satisfied by any of the practical NICs. Therefore, the h parameters of a practical NIC must satisfy conditions of set I in one of its orientations. For convenience, the conditions in set I can be summarized as

$$h_{11} > 0, \quad h_{22} > 0, \quad \Delta h < 0$$

All h parameters here are considered to be real.

To justify the stability statement of the practical NIC by the frequency-dependent linear-network approach, the practical NIC will be considered as having the h matrix

$$[H] = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix}$$

where each h parameter is a real constant. The compensation of parasitic parameters h_{11} and h_{22} will be taken into consideration later. When the

practical NIC is terminated in immittances Z_1 and Y_2 as shown in Figure 32, the input immittances at port 1 and 2 will be respectively

$$Z_{i1} = \frac{h_{11}h_{22} - h_{12}h_{21} + h_{11}Y_2}{h_{22} + Y_2} \tag{56}$$

$$Y_{i2} = \frac{h_{11}h_{22} - h_{12}h_{21} + h_{22}Z_1}{h_{11} + Z_1} \tag{57}$$

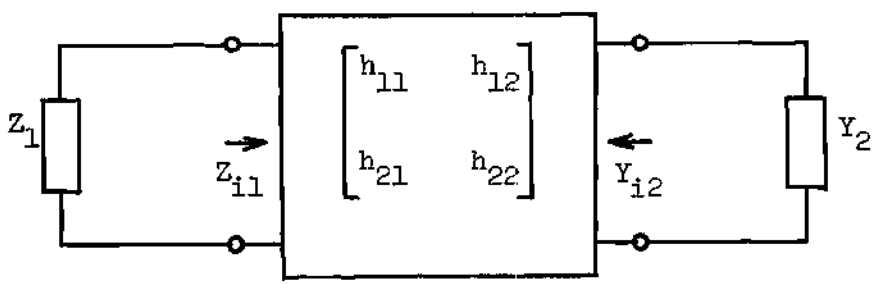


Figure 32. A Terminated Practical NIC.

Generally, the immittances Z_1 and Y_2 are positive-real rational functions

$$Z_1 = \frac{N_1(s)}{D_1(s)} \tag{58}$$

$$Y_2 = \frac{N_2(s)}{D_2(s)} \tag{59}$$

By substituting Equations (58) and (59) into (56) and (57), the input

immittances become

$$Z_{i1} = \frac{\Delta h + h_{11}N_2(s)}{h_{22}D_2(s) + N_2(s)} \tag{60}$$

$$Y_{i2} = \frac{\Delta h + h_{22}N_1(s)}{h_{11}D_1(s) + N_1(s)} \tag{61}$$

From Equations (60) and (61), it can easily be seen that both denominators are Hurwitz polynomials because h_{11} and h_{22} are positive real numbers, and $N_1(s)$, $D_1(s)$, $N_2(s)$, and $D_2(s)$ are all Hurwitz polynomial.[19] Therefore, both Z_{i1} and Y_{i2} cannot have right-half-plane poles and port 1 is OCS; port 2 is SCS. Also, from Equations (60) and (61), it can easily be recognized that both numerators are not Hurwitz polynomials because the coefficients of both constant terms are negative. Both Z_{i1} and Y_{i2} have right-half-plane zeros and therefore, port 1 is SCU and port is OCU. It should be noted that the addition of compensation networks to idealize the practical NIC does not change the form of Equations (56) and (57), because the compensation networks can be included in the immittances Z_1 and Y_2. Therefore, the conclusion derived above is also applicable to a fully compensated ideal NIC.

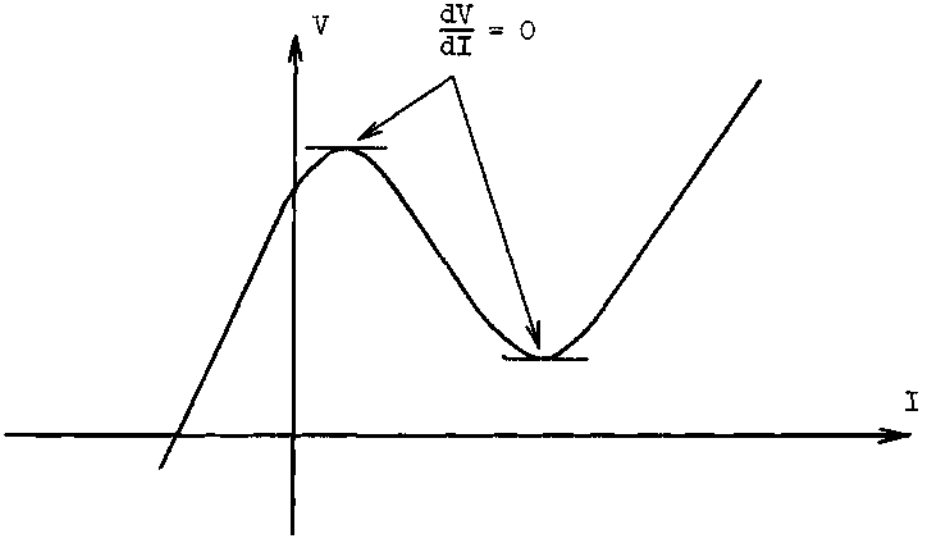
The second approach to justify the stability statement of the NIC is to consider the practical NIC as a nonlinear device. The input impedance of an NIC is a negative resistance when a resistor is connected to its output port. Since a negative resistance can be considered a source of energy, and since any physically realizable source can supply only a

finite amount of energy, the negative resistance can exist only within a limited region of its voltage-current (v-i) characteristic.[18] This non-linearity of the NIC can also be deduced from the fact that the NIC are realized by controlled sources, and that all practical controlled sources are linear only within a limited region of the v-i plane. Thus, the input v-i characteristic at a port of a practical NIC, when the other port is terminated in a resistor, can be assumed to have at least three sections -- a negative-resistance section in the middle and a positive-resistance section at each end. This type of negative resistance can be classified as either current-controlled or voltage-controlled as shown in Figure 33. For a current-controlled negative resistance, there is only one value of voltage for any specified current, and the derivative dv/di at both turning points are zero. For a voltage-controlled negative resistance, there is only one value of current at any specified voltage, and the derivative dv/di at both turning points are infinity.

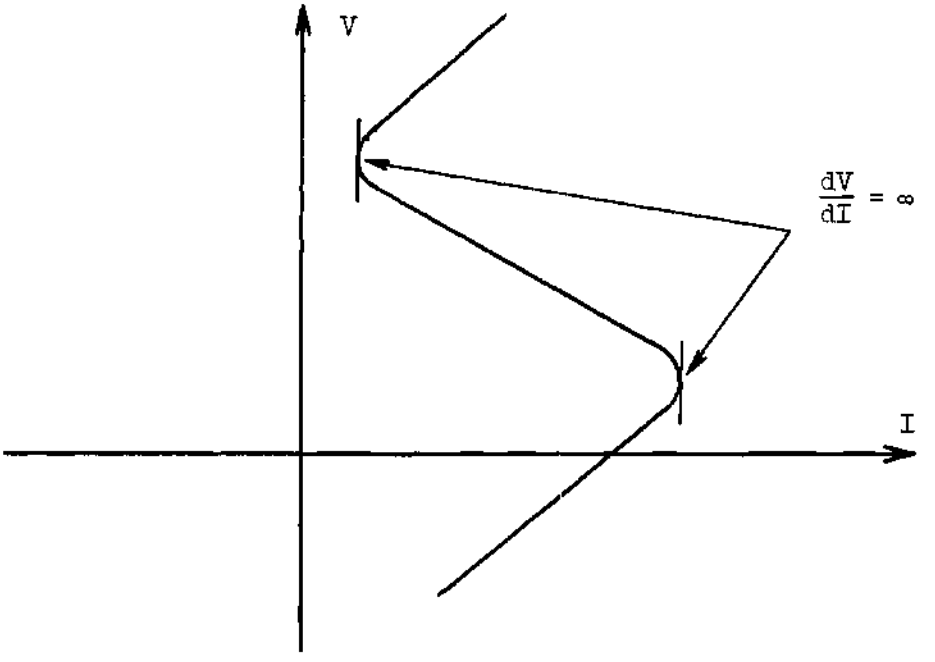
Consider again the terminated practical NIC circuit of Figure 32, with the impedance Z_1 replaced by a resistance r_1 and the admittance Y_2 replaced by a conductance g_2, the input resistance at both ports are given by

$$R_{i1} = \frac{dv_1}{di_1} = \frac{h_{11}h_{22} - h_{12}h_{21} + h_{11}g_2}{h_{22} + g_2} \tag{62}$$

$$R_{i2} = \frac{dv_2}{di_2} = \frac{h_{11} + r_1}{h_{11}h_{22} - h_{12}h_{21} + h_{22}r_1} \tag{63}$$



(a)



(b)

Figure 33. (a) Current-Controlled -R.
(b) Voltage-Controlled -R.

When the practical NIC is functioning within section II of the v-i characteristic in Figure 33, the practical NIC is fully compensated and operating as an ideal NIC. The compensation resistors are included in the terms of r_1 and g_2. As the operation region of the NIC moves from section II toward I or III, the parameters h_{11}, h_{12}, h_{21}, and h_{22} will change in such a way that the input resistance will change from negative to positive. Since h_{11}, h_{22}, r_1, and g_2 are all positive, only the numerator of R_{i1} and the denominator of R_{i2} can become zero. In other words, R_{i1} can only go through zero and R_{i2} can only go through infinity as they change signs. Therefore, if R_{i1} is current-controlled then R_{i2} must be voltage-controlled or vice versa. In other words, if port 1 is OCS-SCU, then port 2 must be SCS-OCU; or vice versa.

The results on the stability properties of the NIC, derived from the two analyses above with different approaches, have led to the same conclusion. Accordingly, all the NICs obtained in this research should be OCS-SCU at <u>port 1</u> and SCS-OCU at <u>port 2</u>. This conclusion has been experimentally confirmed. Figure 34 shows the arrangements for stability studies. Experimental results have shown that the NIC will be oscillating if

$$|R_s| > |R_i| \tag{64}$$

for an OCU port and

$$|R_s| < |R_i| \tag{65}$$

for a SCU port. Figure 35 shows the voltage wave forms at different points of the circuit when the NIC is oscillating. The one at the top is the voltage wave form across the resistor R_s. The middle one is the voltage across capacitor C_3, and the bottom one is the voltage at the input port of the NIC.

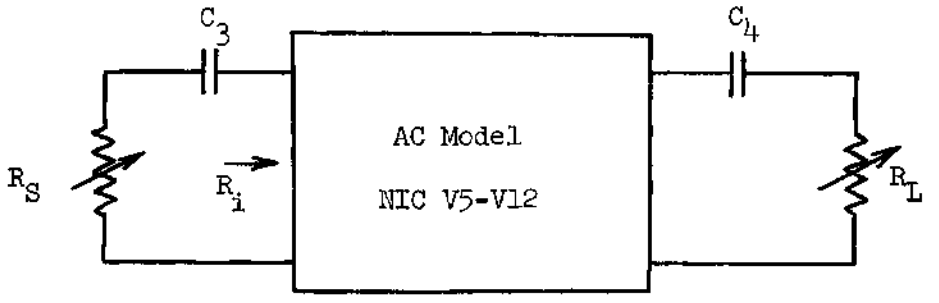


Figure 34. Arrangements for the Stability Study.

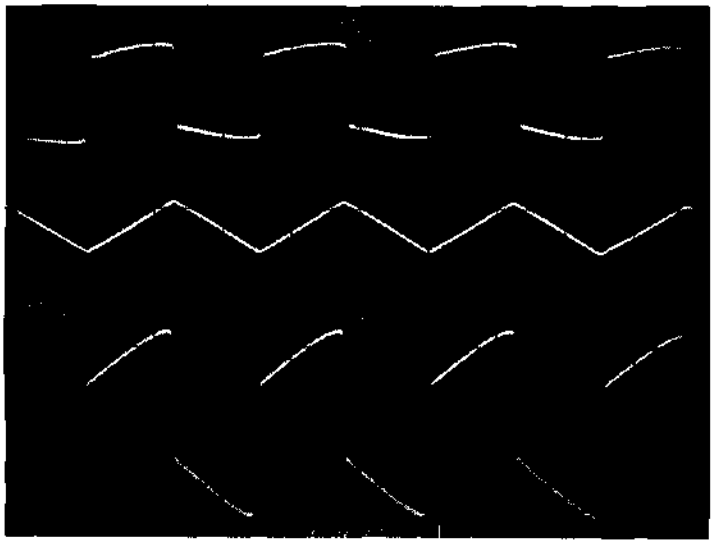


Figure 35. Voltage Wave Forms of an Oscillating NIC.

CHAPTER V

THE NEGATIVE-RESISTANCE CIRCUITS

The negative resistance is widely known for its utilization in amplifiers, oscillators and logic circuits. More recently, negative resistances are employed in network synthesis[20] and in the realization of active elements.[21] For practical applications, the negative resistance is considered a building block which can be in the form of a physical device such as the tunnel diode or in the form of circuitries such as NICs or -R circuits. Although a negative resistance can readily be obtained by terminating an NIC in a resistor, this is not always an economical scheme since a negative-resistance is a one-port device while an NIC is a two-port device. From a practical point of view, a negative-resistance circuit is usually easier to bias and less complex in its practical form than the corresponding NIC. For this reason, all -R circuits will be identified from the NICs realized in this research.

Since the negative resistance realized from an NIC is current-controlled at one port and voltage-controlled at the other port, an NIC can be used to produce both types of negative resistances.

Two basic negative-resistance circuits can be derived from any one of the basic nonideal NICs listed in Tables 3, 4 and 5, by terminating each of its two ports in a resistor. The negative resistance so obtained is current-controlled if port 1 is the input port, and voltage-controlled if port 2 is the input one. Tables 6, 7 and 8 respectively list all the negative-resistance circuits of all FETs, all transistors, and combinations

of FET and transistor.

The development of a basic negative-resistance circuit into its operational form is similar to those discussed in Chapter III for a non-ideal NIC. No more elaboration on this subject will be given here. Rather, some examples of negative-resistance circuits with their v-i characteristic curves plotted as a function of the terminated-load resistance are presented.

Figures 36 and 37 show two all-FET negative-resistance circuits, derived from basic NIC V5-V12, with their v-i characteristic curves. Figure 38 shows an all-transistor negative-resistance circuit, derived from basic NIC I6′-I1, with its v-i characteristic curve. Figure 39 shows a negative-resistance circuit containing a FET and a transistor, derived from basic NIC V2-V12, with its characteristic curves.

Table 6. Basic FET -R Circuits.

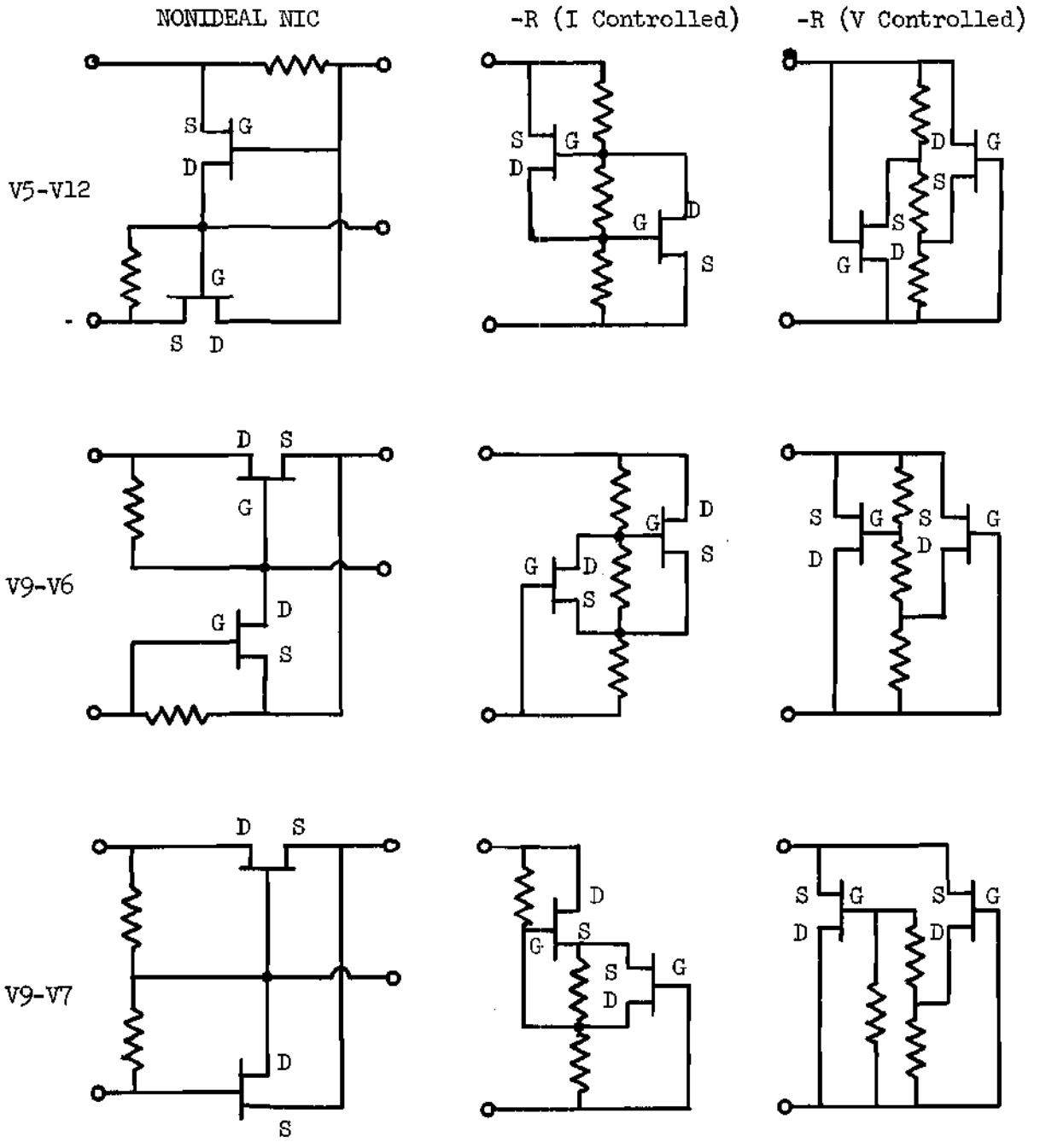


Table 7. Basic Transistor -R Circuits.

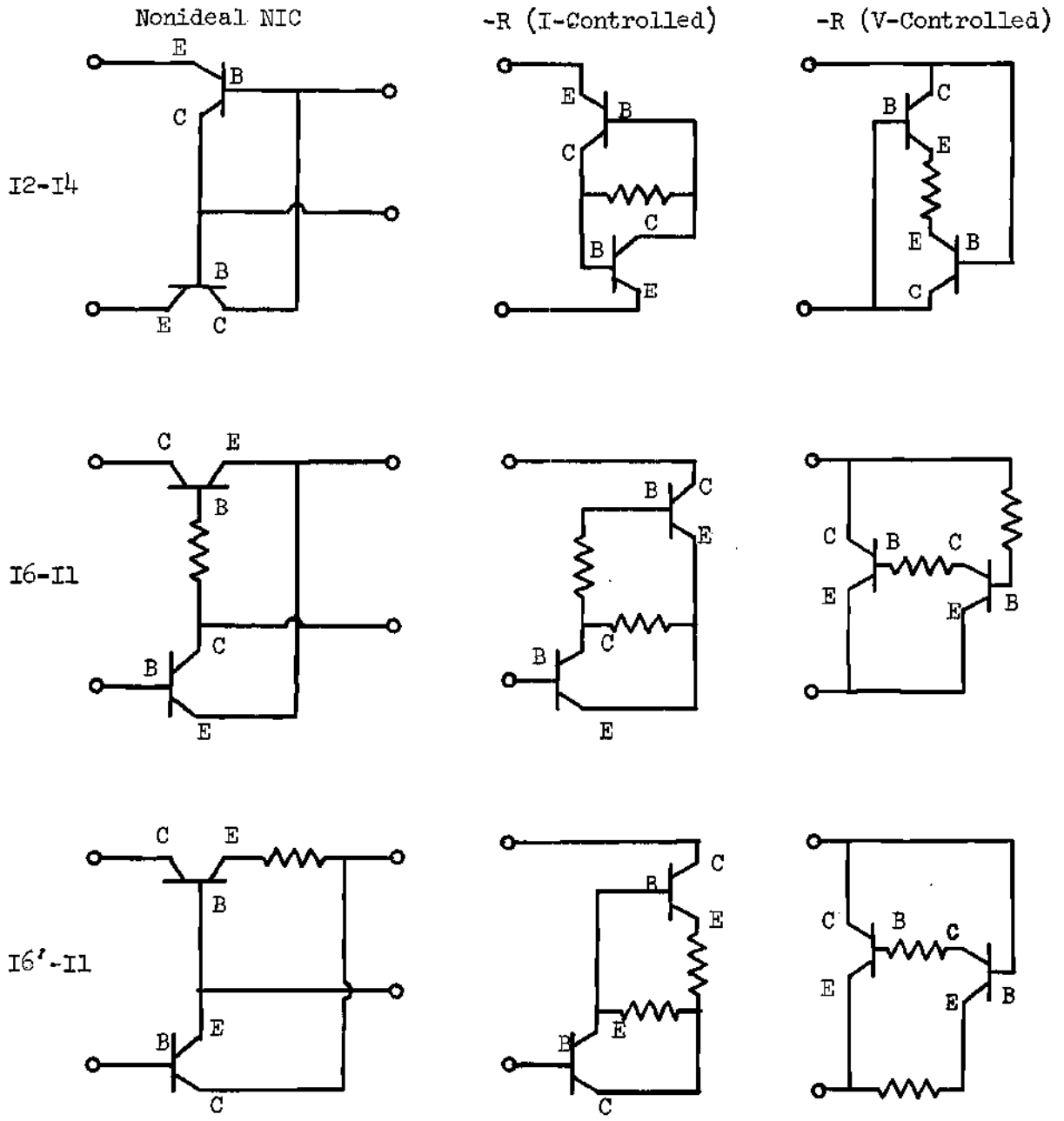
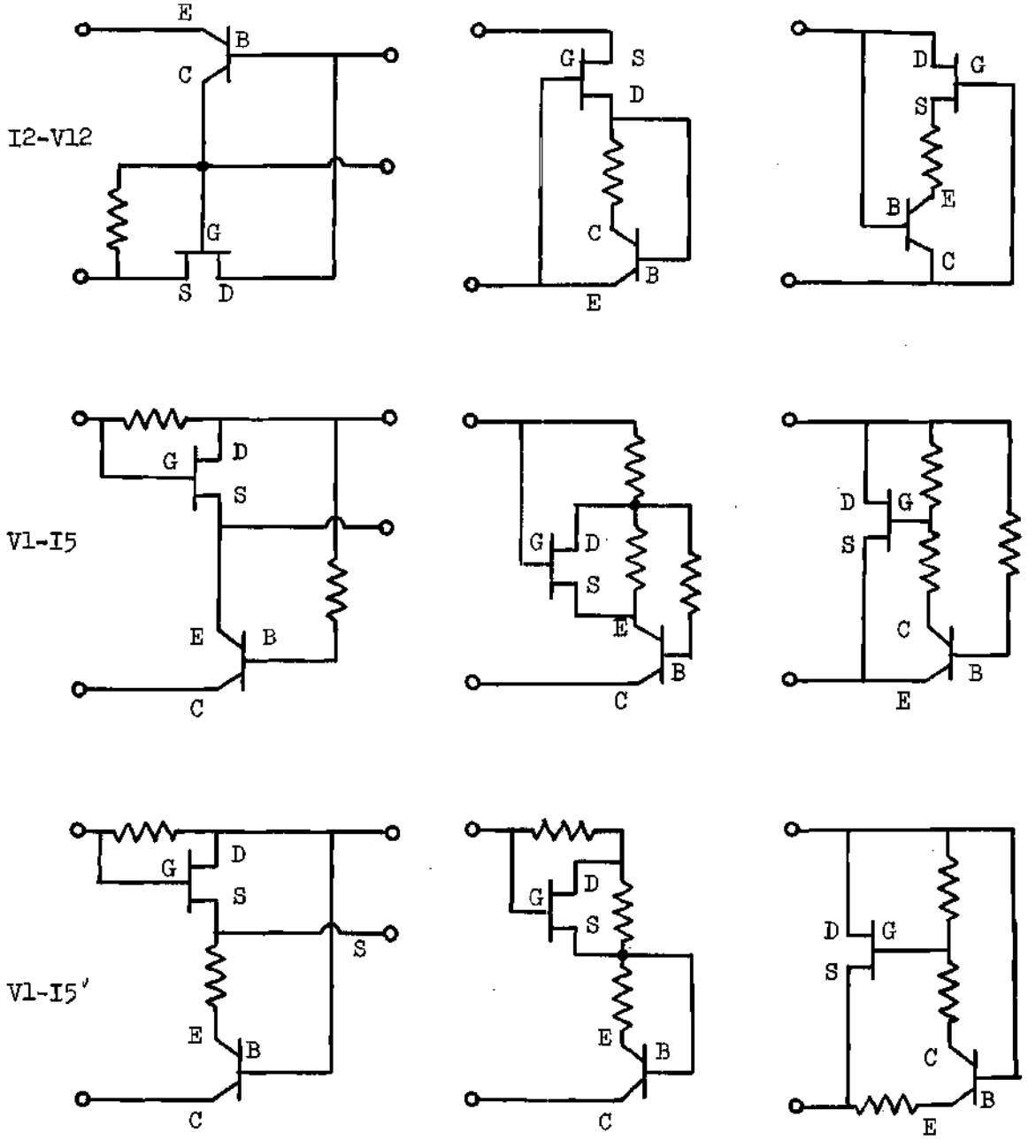
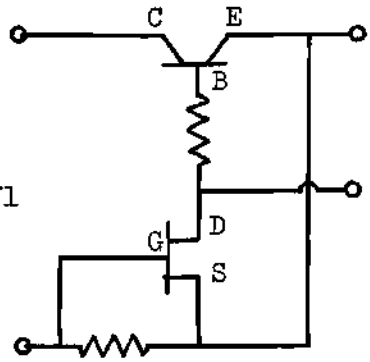
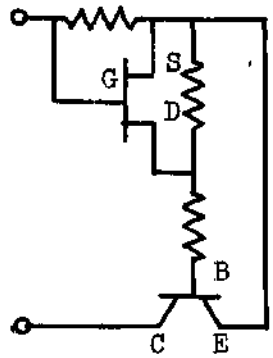


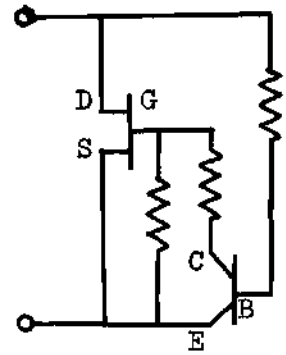
Table 8. Basic Transistor-FET -R Circuits.



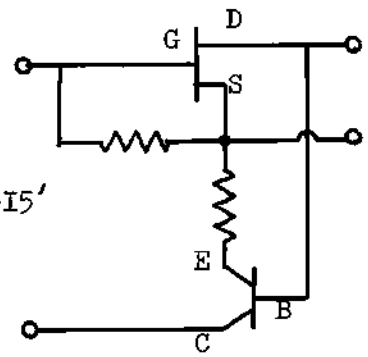
I6-V1

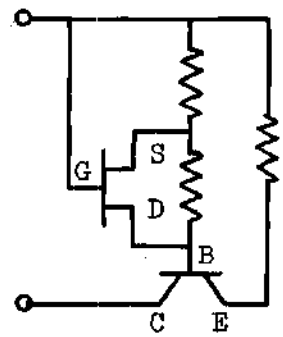


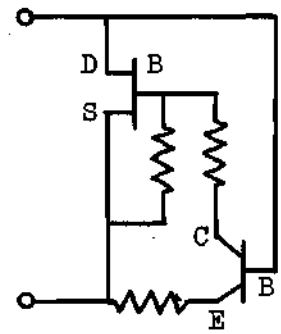




V11-I5'







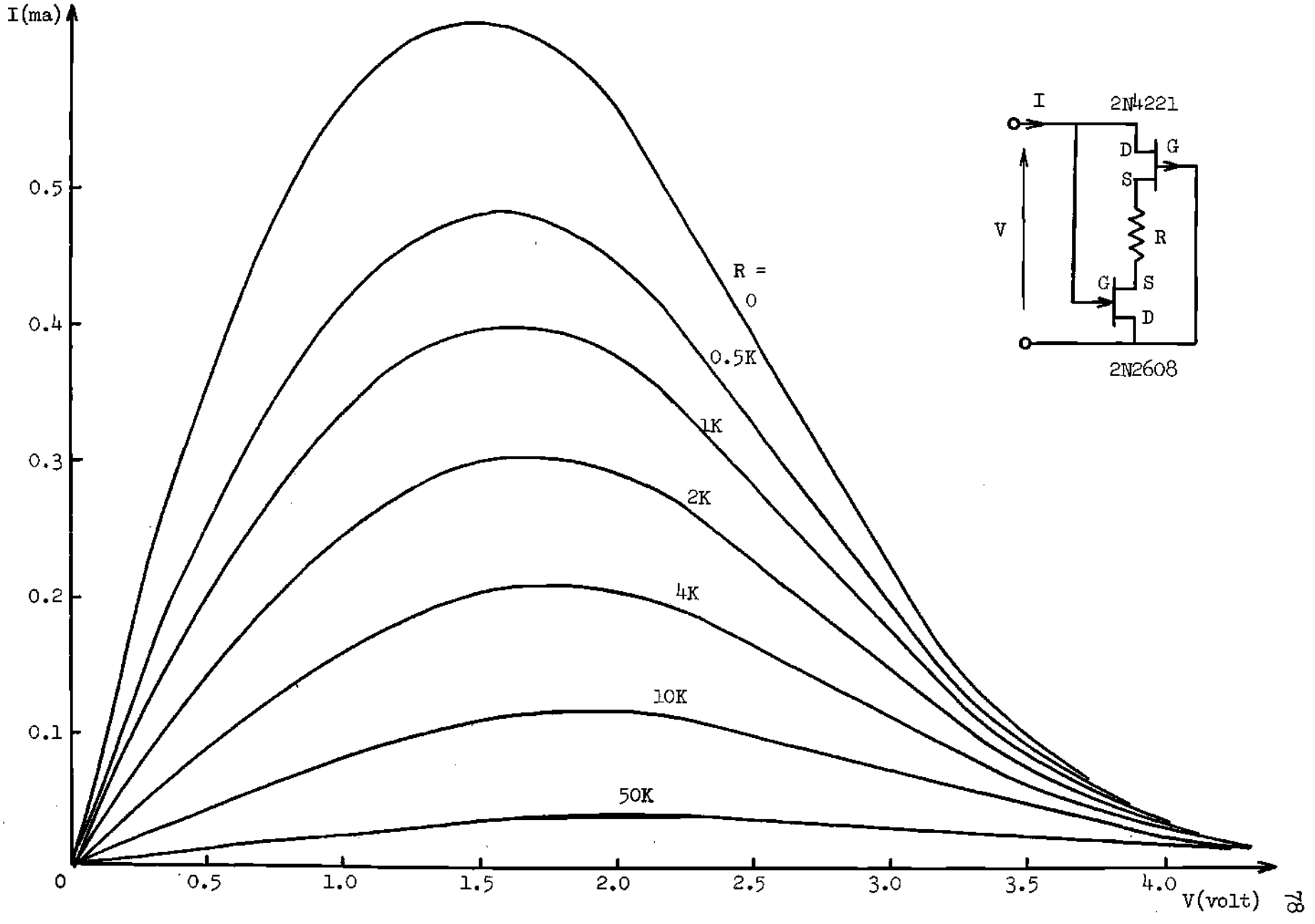


Figure 36. FET Voltage-Controlled -R of V5-V12.

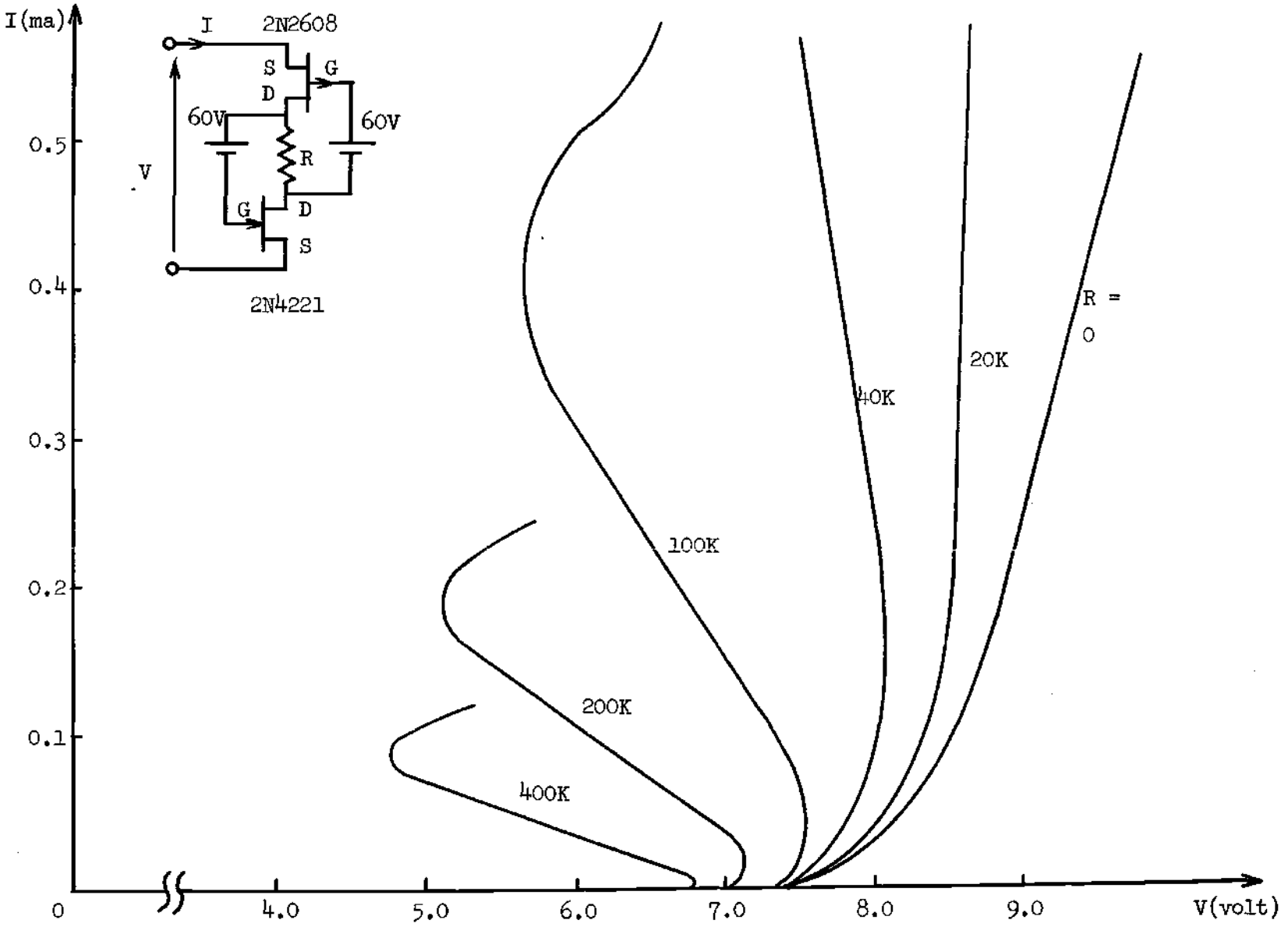


Figure 37. FET Current-Controlled -R of V5-V12.

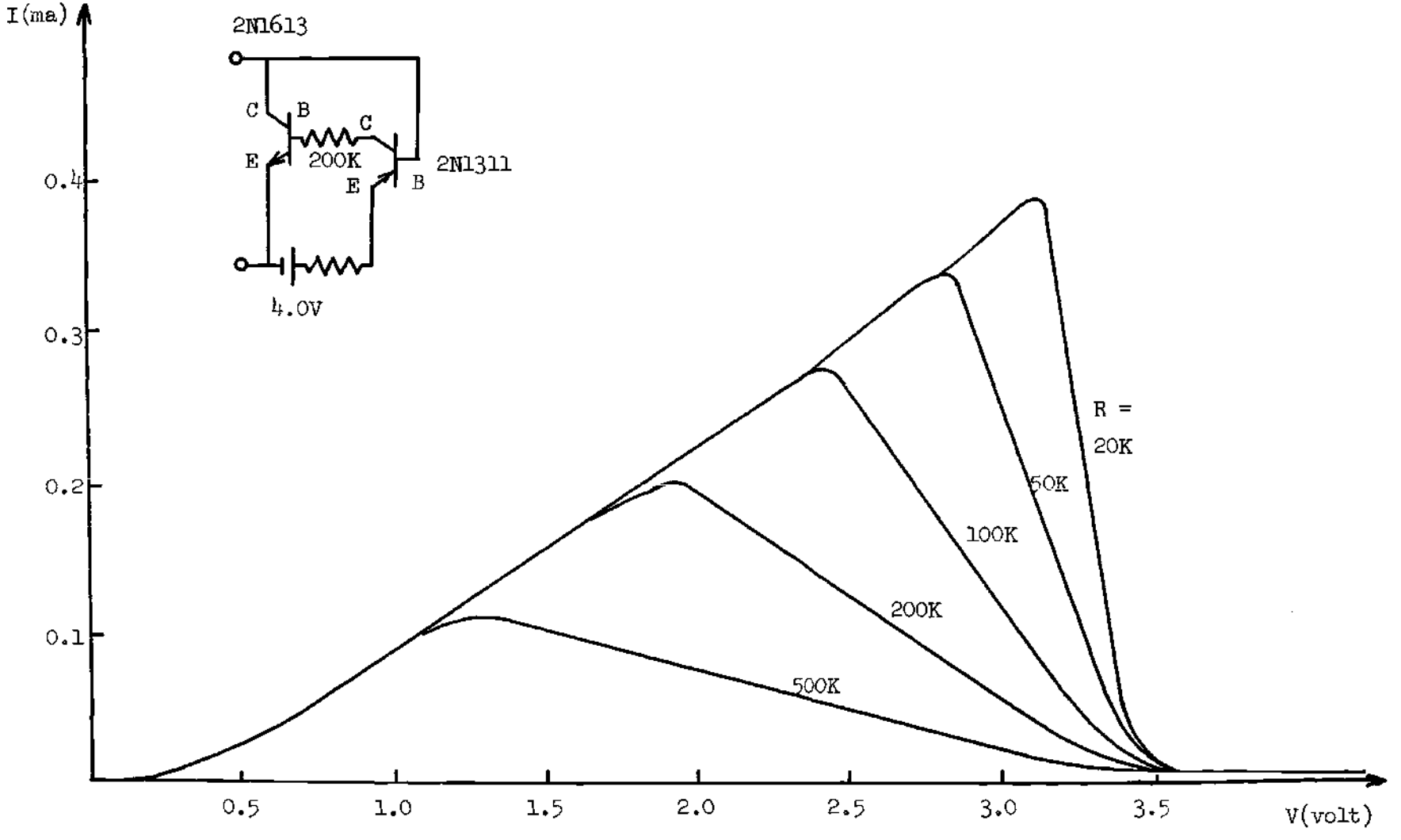


Figure 38. Transistor Voltage-Controlled -R of I6'-I1.

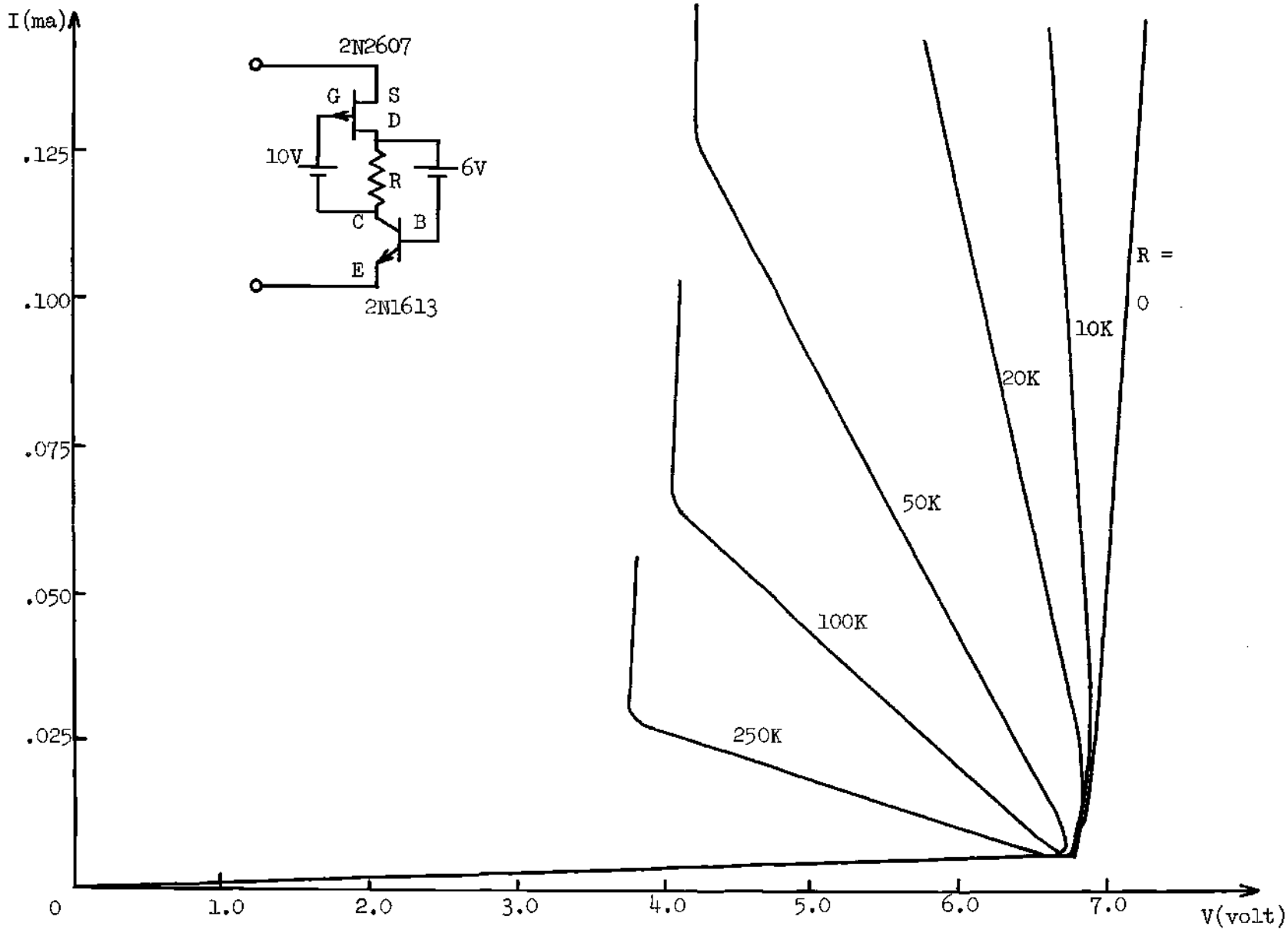


Figure 39. Transistor-FET Current-Controlled -R of I2-V12.

CHAPTER VI

CONCLUSIONS

In this research, the nonideal NIC has been mathematically defined. The criteria under which a two-port can be considered a nonideal NIC have been derived respectively for a two-port with complex parameters and for a two-port with real parameters. By applying these criteria, techniques have been developed to interconnect two elementary networks and many basic NIC circuits have been successfully realized using FETs and junction transistors. Of the eleven basic NICs realized in this research, NIC I2-I4 is the only one that has been proposed prior to this report.[4]

An example was given on the development of a basic nonideal NIC into a practical ac model NIC and a dc model NIC. The performance of both ac and dc models are satisfactory. The frequency response of the NICs built is ideal (no phase shift) up to 100 kHz. In building the circuits, no special care was taken to improve the frequency response. With the selection of better quality active devices and the minimization of stray circuit capacitances and inductances, the practical NICs should operate into the MHz ranges.

The number of active devices used in each NIC has been limited to the minimum which is two. By increasing the number of active devices in each NIC or in each elementary network, there is no doubt that more NICs can be found using the same technique developed in this research. The complexity of realization will increase as the number of active devices in each NIC is increased.

The stability problem of the NIC has been analyzed in this research with two new approaches. The new approaches not only prove that an NIC is SCS-OCU at one port and OCS-SCU at the other, but also predict which port of the NIC is SCS-OCU and which is OCS-SCU. In discussing the stability problem of a compensated ideal NIC, the compensation networks are considered parts of the terminating immittances, and the compensated NIC has the same basic stability properties as the nonideal one. It should be pointed out that the above reasoning is valid only if the compensated NIC is itself stable. It is possible that the compensation networks might cause the NIC to become unstable. This is because the parallel compensation network is in parallel with the SCU port and the series compensation network is in series at the OCU port. These compensation networks respectively control the highest terminating impedance at the SCU port and the lowest series impedance at the OCU port of a practical NIC. The smaller the parasitic parameters h_{11} and h_{22}, the smaller the immittance of the compensation networks and the better the quality of the nonideal NIC.

Current-controlled and voltage-controlled negative-resistance circuits have been derived from each nonideal NIC. A total of twenty-two negative resistance circuits have been found; half of them are current-controlled, and the other half are voltage-controlled. Of all the negative-resistance circuits obtained in this research, current stable -R circuit of V5-V12 is the only one that has been reported by others earlier.[9]

APPENDICES

APPENDIX I

DERIVATION OF MATRIX FOR THE COMPENSATED NIC

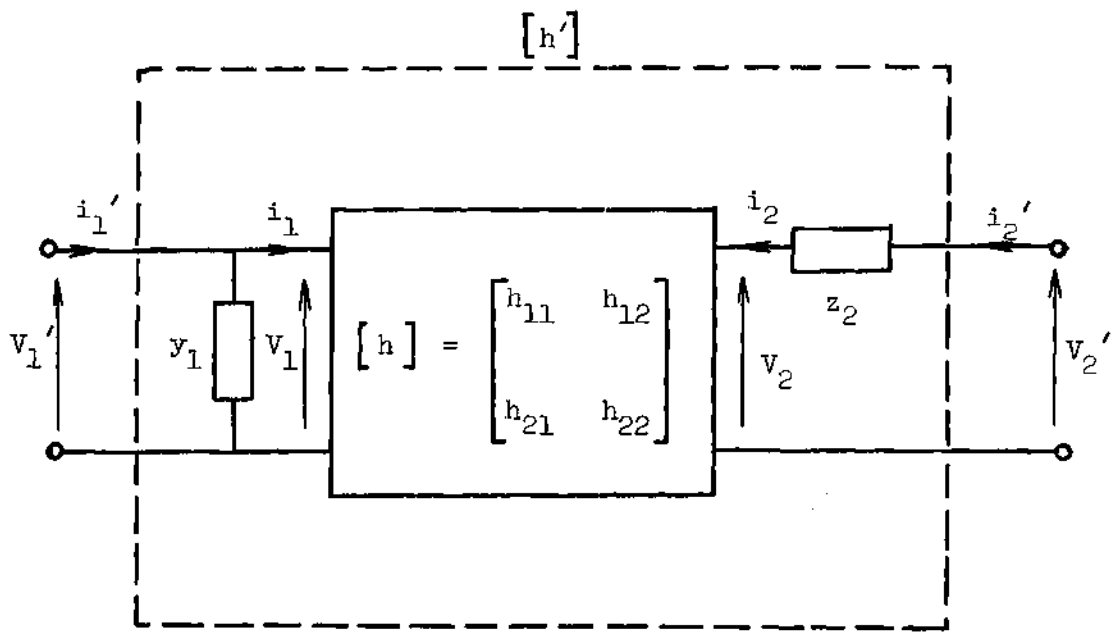


Figure A1. The Compensation of a Nonideal NIC.

$$V_1 = h_{11}i_1 + h_{12}V_2 \tag{A1}$$

$$i_2 = h_{21}i_2 + h_{22}V_2 \tag{A2}$$

From Figure A1, it can be found

$$V_1 = V_1' \tag{A3}$$

$$i_1 = i_1' - y_1 V_1 \tag{A4}$$

$$V_2 = V_2' - z_2 i_2 \tag{A5}$$

$$i_2 = i_2' \tag{A6}$$

Substitute (A3), (A4), (A5) and (A6) into (A1) and (A2),

$$V_1' = h_{11}(i_1' - y_1 V_1') + h_{12}(V_2' - z_2 i_2') \tag{A7}$$

$$i_2' = h_{21}(i_1' - y_1 V_1') + h_{22}(V_2' - z_2 i_2') \tag{A8}$$

Rearrange (A7) and (A8)

$$V_1' = \frac{h_{11}}{1 + h_{11} y_1} i_1' + \frac{h_{12}}{1 + h_{11} y_1} V_2' - \frac{h_{12} z_2}{1 + h_{11} y_1} i_2' \tag{A9}$$

$$i_2' = \frac{h_{21}}{1 + h_{22} z_2} i_1' + \frac{h_{22}}{1 + h_{22} z_2} V_2' - \frac{h_{21} y_1}{1 + h_{22} z_2} V_1' \tag{A10}$$

Substitute (A10) into (A9)

$$V_1' = \frac{h_{11}(1 + h_{22}z_2) - h_{12}h_{21}z_2}{(1 + h_{11}y_1)(1 + h_{22}z_2) - h_{12}h_{21}y_1z_2} i_1' \qquad (A11)$$

$$+ \frac{h_{12}(1 + h_{22}z_2) - h_{12}h_{22}z_2}{(1 + h_{11}y_1)(1 + h_{22}z_2) - h_{12}h_{21}y_1z_2} V_2'$$

Let

$$\Delta h = h_{11}h_{22} - h_{12}h_{21}$$

(A11) becomes

$$V_1' = \frac{h_{11} + z_2\Delta h}{1 + h_{11}y_1 + h_{22}z_2 + y_1z_2\Delta h} i_1 \qquad (A12)$$

$$+ \frac{h_{12}}{1 + h_{11}y_1 + h_{22}z_2 + y_1z_2\Delta h}$$

Substitute (A12) into (A10)

$$i_2' = \frac{h_{21}}{1 + h_{11}y_1 + h_{22}z_2 + y_1z_2\Delta h} i_1' \qquad (A13)$$

$$+ \frac{h_{22} + y_1\Delta h}{1 + h_{11}y_1 + h_{22}z_2 + y_1z_2\Delta h}$$

Therefore

$$\begin{bmatrix} h_{11}' & h_{12}' \\ h_{21}' & h_{22}' \end{bmatrix} = \begin{bmatrix} \dfrac{h_{11} + z_2\Delta h}{1 + h_{11}y_1 + h_{22}z_2 + y_1z_2\Delta h} & \dfrac{h_{12}}{1 + h_{11}y_1 + h_{22}z_2 + y_1z_2\Delta h} \\ \dfrac{h_{21}}{1 + h_{11}y_1 + h_{22}z_2 + y_1z_2\Delta h} & \dfrac{h_{22} + y_1\Delta h}{1 + h_{11}y_1 + h_{22}z_2 + y_1z_2\Delta h} \end{bmatrix} \quad \text{(A14)}$$

APPENDIX II

A PROOF TO ELIMINATE SERIES-SERIES AND PARALLEL-PARALLEL INTERCONNECTIONS AS POSSIBLE WAYS OF OBTAINING NICS

Some matrix transformation equations which will be used in this proof are listed in the following.

$$\begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} = \begin{bmatrix} \frac{\Delta h}{h_{22}} & \frac{h_{12}}{h_{22}} \\ -\frac{h_{21}}{h_{22}} & \frac{1}{h_{22}} \end{bmatrix} \tag{A15}$$

$$\begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} = \begin{bmatrix} \frac{\Delta z}{z_{22}} & \frac{z_{12}}{z_{22}} \\ -\frac{z_{21}}{z_{22}} & \frac{1}{z_{22}} \end{bmatrix} \tag{A16}$$

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} \frac{1}{h_{11}} & -\frac{h_{12}}{h_{11}} \\ \frac{h_{21}}{h_{11}} & \frac{\Delta h}{h_{11}} \end{bmatrix} \tag{A17}$$

$$\begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} = \begin{bmatrix} \frac{1}{y_{11}} & -\frac{y_{12}}{y_{11}} \\ \frac{y_{21}}{y_{11}} & \frac{\Delta y}{y_{11}} \end{bmatrix} \tag{A18}$$

where

$$\Delta h = h_{11}h_{22} - h_{12}h_{21}$$

$$\Delta z = z_{11}z_{22} - z_{12}z_{21}$$

$$\Delta y = y_{11}y_{22} - y_{12}y_{21}$$

By considering two practical elementary networks as having z matrices of respectively [z′] and [z″], y matrices of [y′] and [y″], and h matrices of [h′] and [h″], the matrices of series-series and parallel-parallel interconnected networks will respectively be

$$\begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} = \begin{bmatrix} z_{11}' + z_{11}'' & z_{12}' + z_{12}'' \\ z_{21}' + z_{21}'' & z_{21}' + z_{21}'' \end{bmatrix} \tag{A19}$$

and

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} y_{11}' + y_{11}'' & y_{12}' + y_{12}'' \\ y_{21}' + y_{21}'' & y_{21}' + y_{21}'' \end{bmatrix} \tag{A20}$$

From Table I and II hybrid h parameters of all elementary networks satisfy

$$h_{11}' \geq 0, \quad h_{22}' > 0, \quad \Delta h' \geq 0 \tag{A21}$$

By substituting (A21) into (A15) and (A17), conditions of (A21) can be expressed in z and y parameters as

$$z_{11}' \geq 0, \quad z_{22}' \geq 0, \quad \Delta z' = \frac{h_{11}'}{h_{22}'} \geq 0 \tag{A22}$$

$$y_{11}' \geq 0, \quad y_{22}' \geq 0, \quad \Delta y' = \frac{h_{22}}{h_{11}} \geq 0 \tag{A23}$$

From (A19), (A20), (A22) and (A23), parameters of series-series and parallel-parallel interconnected networks can easily be found to respectively satisfy

$$z_{11} \geq 0 \quad , \quad z_{22} \geq 0 \tag{A24}$$

and

$$y_{11} \geq 0 \quad , \quad y_{22} \geq 0 \tag{A25}$$

By substituting (A24) and (A25) respectively into (A16) and (A18), it can be observed that for both interconnected networks

$$h_{22} \geq 0 \tag{A26}$$

The only set of nonideal NIC conditions which can be satisfied by (A26) is the set I or

$$h_{11} \geqq 0, \quad h_{22} \geqq 0 \tag{14}$$

$$\Delta h \leqq 0 \tag{15}$$

$$h_{12}h_{22} > 0 \tag{16}$$

But from (A24) and (A16)

$$\Delta h = \frac{z_{11}}{z_{22}} \geqq 0 \tag{A27}$$

and from (A25) and (A18)

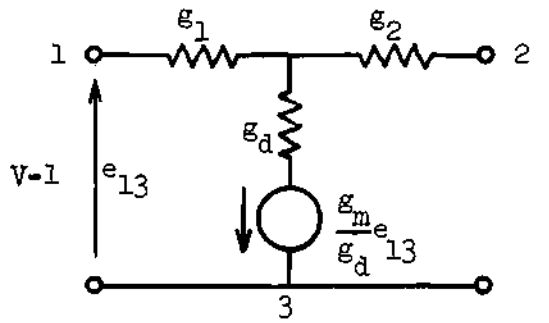
$$\Delta h = \frac{y_{22}}{y_{21}} \geqq 0 \tag{A28}$$

Equation (15) is violated in both cases; therefore, series-series and parallel-parallel interconnection of two elementary networks will not lead to a nonideal NIC.

APPENDIX III

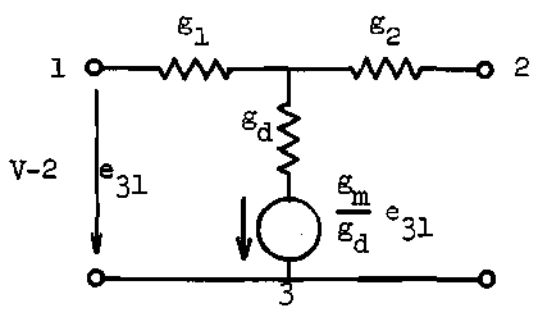
ELEMENTARY NETWORKS WITH A VOLTAGE-CONTROLLED SOURCE

V-1



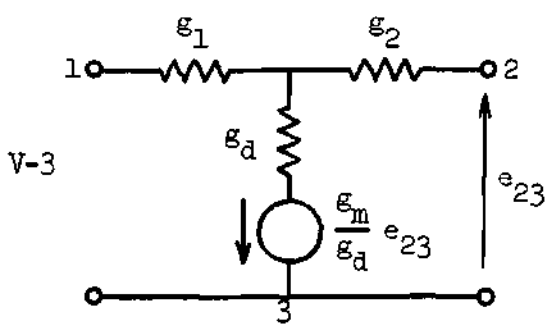
$$\begin{bmatrix} \frac{g_1+g_2+g_d}{g_1(g_2+g_m+g_d)} & \frac{g_2}{(g_2+g_m+g_d)} \\ \frac{g_2(g_m-g_1)}{g_1(g_2+g_m+g_d)} & \frac{g_2(g_m+g_d)}{(g_2+g_m+g_d)} \end{bmatrix}$$

V-2



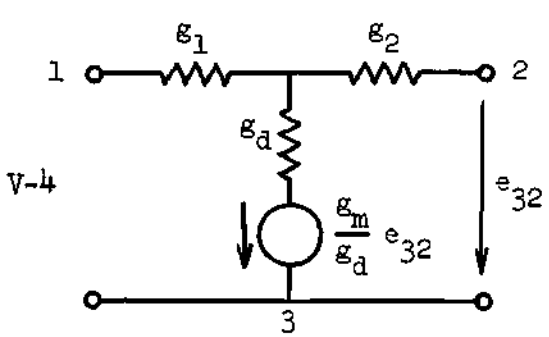
$$\begin{bmatrix} \frac{g_1+g_2+g_d}{g_1(g_2+g_d-g_m)} & \frac{g_2}{g_2+g_d-g_m} \\ \frac{-g_2(g_1+g_m)}{g_1(g_2+g_d-g_m)} & \frac{g_2(g_d-g_m)}{(g_2+g_d-g_m)} \end{bmatrix}$$

V-3



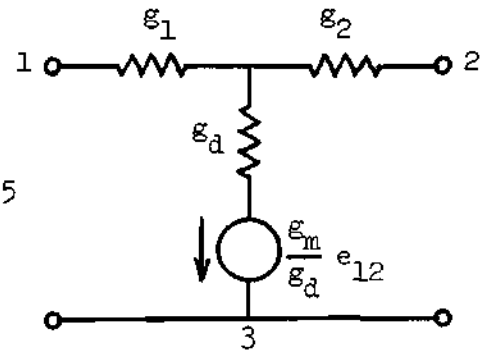
$$\begin{bmatrix} \frac{g_1+g_2+g_d}{g_1(g_2+g_d)} & \frac{g_m-g_2}{g_2+g_d} \\ -\frac{g_2}{g_2+g_d} & \frac{g_2(g_m+g_d)}{g_2+g_d} \end{bmatrix}$$

V-4



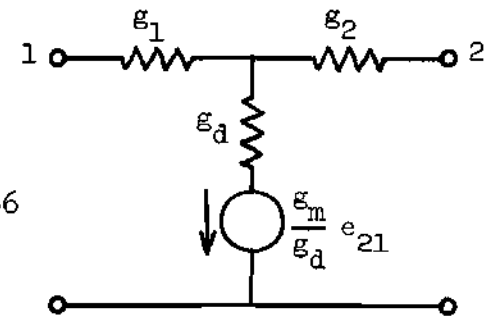
$$\begin{bmatrix} \frac{g_1+g_2+g_d}{g_1(g_2+g_d)} & \frac{g_2+g_m}{g_2+g_d} \\ -\frac{g_2}{g_2+g_d} & \frac{g_2(g_d-g_m)}{g_2+g_d} \end{bmatrix}$$

V-5



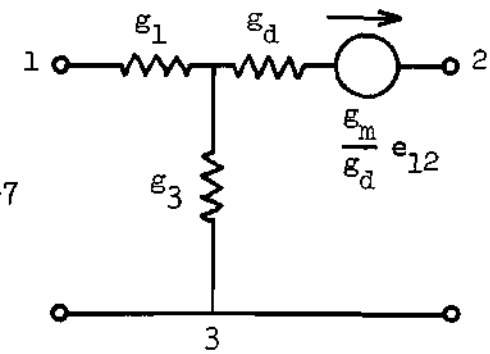
$$\begin{bmatrix} \frac{g_1+g_2+g_d}{g_1(g_2+g_d+g_m)} & \frac{g_2+g_m}{g_2+g_d+g_m} \\ \frac{g_2(g_m-g_1)}{g_1(g_2+g_d+g_m)} & \frac{g_2 g_d}{g_2+g_d+g_m} \end{bmatrix}$$

V-6



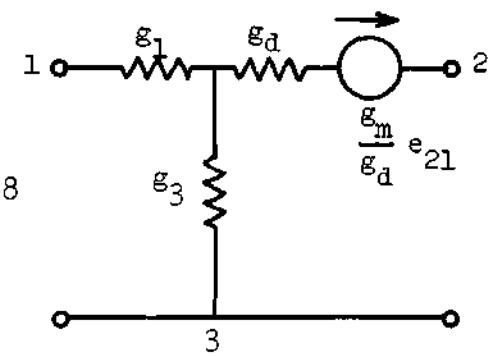
$$\begin{bmatrix} \frac{g_1+g_2+g_d}{g_1(g_2+g_d-g_m)} & -\frac{(g_m-g_2)}{g_2+g_d-g_m} \\ -\frac{g_2(g_1+g_m)}{g_1(g_2+g_d-g_m)} & \frac{g_2 g_d}{g_2+g_d-g_m} \end{bmatrix}$$

V-7



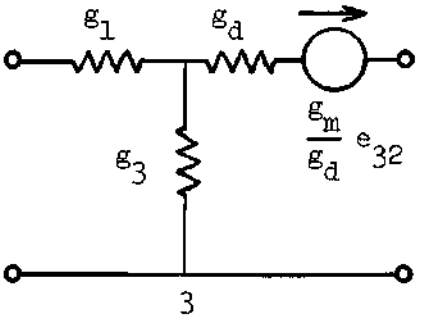
$$\begin{bmatrix} \frac{1}{g_1}+\frac{1}{g_3}-\frac{g_m(g_1+g_3)+g_1 g_d}{g_1 g_3(g_3+g_d+g_m)} & \frac{g_d+g_m}{g_3+g_d+g_m} \\ -\frac{g_1 g_d+g_m(g_1+g_3)}{g_1(g_3+g_d+g_m)} & \frac{g_3(g_d+g_m)}{g_3+g_d+g_m} \end{bmatrix}$$

V-8



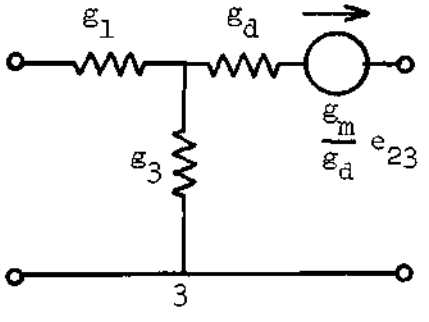
$$\begin{bmatrix} \frac{1}{g_1}+\frac{1}{g_3}+\frac{g_m(g_1+g_3)-g_1 g_d}{y_1 g_3(g_3+g_d-g_m)} & \frac{g_d-g_m}{g_3+g_d-g_m} \\ \frac{g_m(g_1+g_3)-g_1 g_d}{g_1(g_3+g_d-g_m)} & \frac{g_3(g_d-g_m)}{g_3+g_d-g_m} \end{bmatrix}$$

V-9



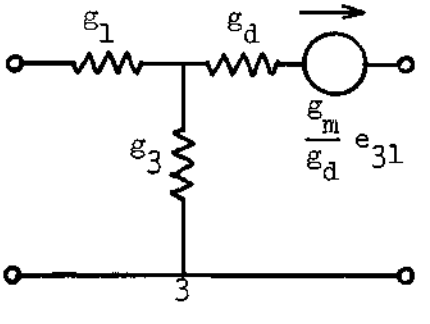
$$\begin{bmatrix} \frac{g_1 - g_3 + g_d}{g_1(g_3+g_d)} & \frac{g_m+g_d}{g_3+g_d} \\ -\frac{g_d}{g_3+g_d} & \frac{g_3(g_m+g_d)}{g_3+g_d} \end{bmatrix}$$

V-10



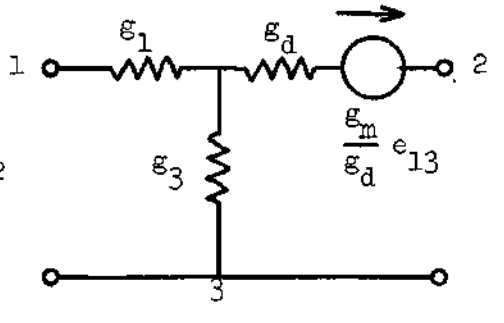
$$\begin{bmatrix} \frac{g_1+g_3+g_d}{g_1(g_3+g_d)} & -\frac{(g_m-g_d)}{g_3+g_d} \\ -\frac{g_d}{g_3+g_d} & \frac{g_3(g_d-g_m)}{g_3+g_d} \end{bmatrix}$$

V-11



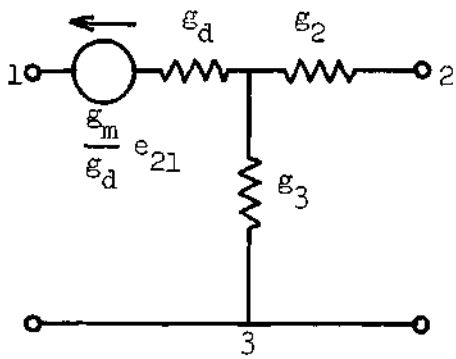
$$\begin{bmatrix} \frac{1}{g_1}+\frac{1}{g_3}+\frac{g_m(g_1+g_3)-g_1g_d}{g_1g_3(g_3+g_d-g_m)} & \frac{g_d}{g_3+g_d-g_m} \\ \frac{g_m(g_1+g_3)-g_1g_d}{g_1(g_3+g_d-g_m)} & \frac{g_3g_d}{g_3+g_d-g_m} \end{bmatrix}$$

V-12



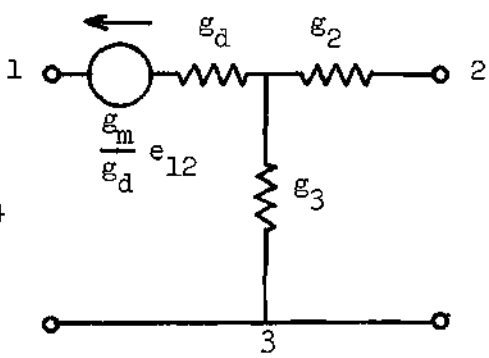
$$\begin{bmatrix} \frac{1}{g_1}+\frac{1}{g_3}-\frac{g_m(g_1+g_3)+g_1g_d}{g_1g_3(g_3+g_m+g_d)} & \frac{g_d}{g_3+g_m+g_d} \\ -\frac{g_m(g_1+g_3)+g_1g_d}{g_1(g_3+g_m+g_d)} & \frac{g_3g_d}{g_3+g_m+g_d} \end{bmatrix}$$

V-13



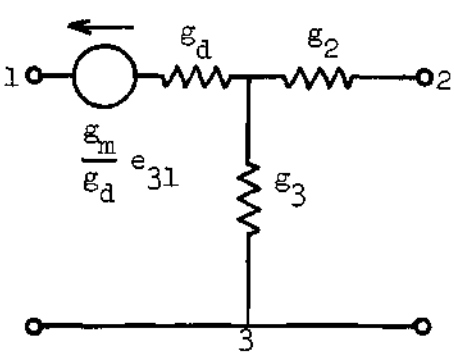
$$\begin{bmatrix} \frac{g_2+g_3+g_d}{(g_2+g_3)(g_d+g_m)} & \frac{g_2g_d+g_m(g_2+g_3)}{(g_2+g_3)(g_d+g_m)} \\ -\frac{g_2}{g_2+g_3} & \frac{g_2g_3}{g_2+g_3} \end{bmatrix}$$

V-14



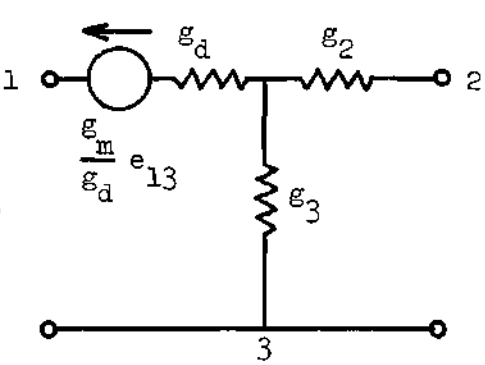
$$\begin{bmatrix} \frac{g_2+g_3+g_d}{(g_2+g_3)(g_d-g_m)} & \frac{g_2g_d-g_m(g_2+g_3)}{(g_2+g_3)(g_d-g_m)} \\ -\frac{g_2}{g_2+g_3} & \frac{g_2g_3}{g_2+g_3} \end{bmatrix}$$

V-15

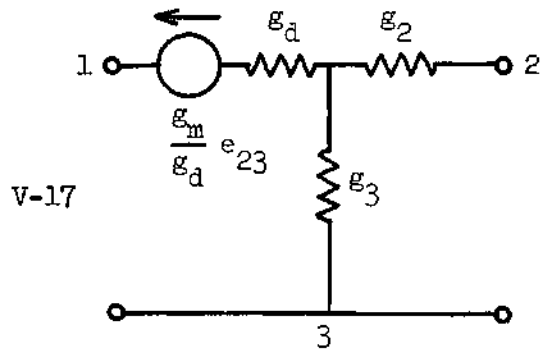


$$\begin{bmatrix} \frac{g_2+g_3+g_d}{(g_2+g_3)(g_d+g_m)} & \frac{g_2g_d}{(g_2+g_3)(g_d+g_m)} \\ -\frac{g_2}{g_2+g_3} & \frac{g_2g_3}{g_2+g_3} \end{bmatrix}$$

V-16

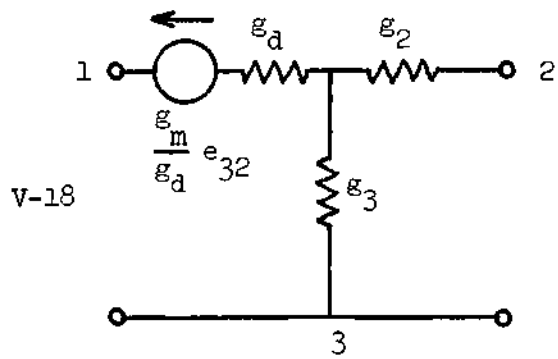


$$\begin{bmatrix} \frac{g_2+g_3+g_d}{(g_2+g_3)(g_d-g_m)} & \frac{g_2g_d}{(g_2+g_3)(g_d-g_m)} \\ -\frac{g_2}{g_2+g_3} & \frac{g_2g_3}{g_2+g_3} \end{bmatrix}$$



V-17

$$\begin{bmatrix} \frac{g_2+g_3+g_d}{g_d(g_2+g_3)} & \frac{g_2g_d+g_m(g_2+g_3)}{g_d(g_2+g_3)} \\ -\frac{g_2}{g_2+g_3} & \frac{g_2g_3}{g_2+g_3} \end{bmatrix}$$



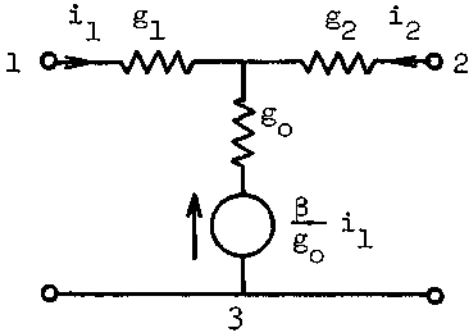
V-18

$$\begin{bmatrix} \frac{g_2+g_3+g_d}{g_d(g_2+g_3)} & \frac{g_2g_d-g_m(g_2+g_3)}{g_d(g_2+g_3)} \\ -\frac{g_2}{g_2+g_3} & \frac{g_2g_3}{g_2+g_3} \end{bmatrix}$$

APPENDIX IV

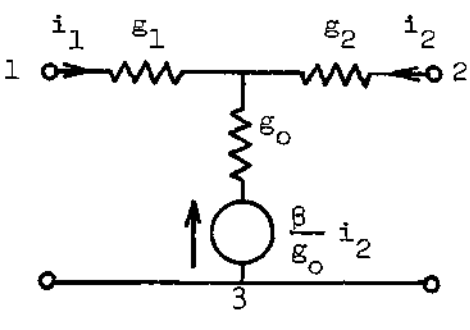
ELEMENTARY NETWORKS WITH A CURRENT-CONTROLLED SOURCE

I-1



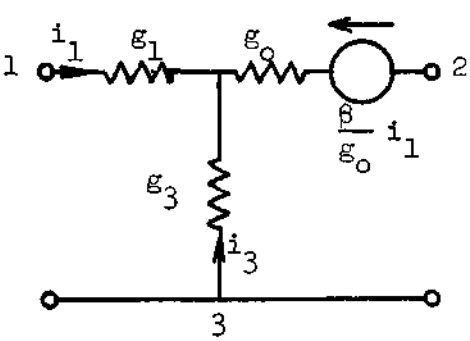
$$\begin{bmatrix} \frac{g_1 g_o(\beta+1)+g_2(g_2+g_o)}{g_1 g_o(g_2+g_o)} & \frac{g_2}{g_2+g_o} \\ -\frac{g_2(\beta+1)}{g_2+g_o} & \frac{g_2 g_o}{g_2+g_o} \end{bmatrix}$$

I-2



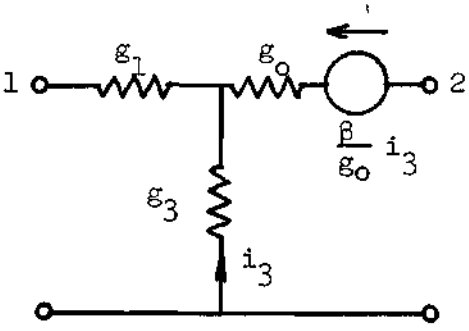
$$\begin{bmatrix} \frac{1}{g_1}+\frac{1}{[g_2(\beta+1)+g_o]} & \frac{g_2(\beta+1)}{[g_2(\beta+1)+g_o]} \\ -\frac{g_2}{[g_2(\beta+1)+g_o]} & \frac{g_2 g_o}{[g_2(\beta+1)+g_o]} \end{bmatrix}$$

I-3



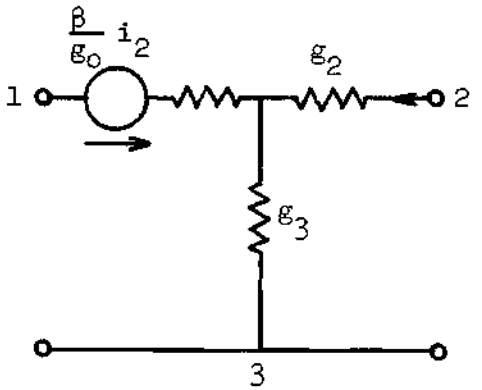
$$\begin{bmatrix} \frac{1}{g_1}+\frac{\beta+1}{g_3+g_o} & \frac{g_o}{g_3+g_o} \\ \frac{g_3\beta}{g_3+g_o} & \frac{g_3 g_o}{g_3+g_o} \end{bmatrix}$$

I-4



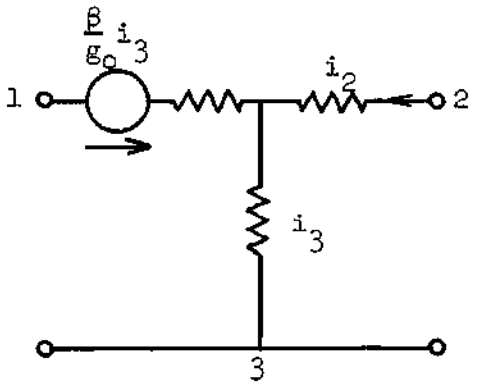
$$\begin{bmatrix} \frac{1}{g_1}+\frac{1}{g_3}-\frac{\beta(g_1+g_o)}{g_1[(\beta+1)g_3+g_o]} & \frac{g_o}{(\beta+1)g_3+g_o} \\ -\frac{g_3(\beta g_1+g_o)}{g_1[(\beta+1)g_3+g_o]} & \frac{g_o g_3}{(\beta+1)g_3+g_o} \end{bmatrix}$$

I-5



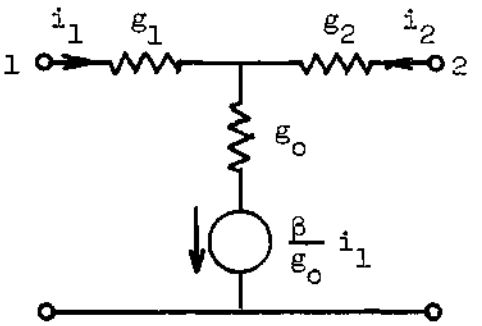
$$\begin{bmatrix} \frac{g_3(\beta g_2+g_3)+g_o g_3}{g_o g_3(g_2+g_3)} & \frac{-\beta g_2 g_3+g_o g_2}{g_o(g_2+g_3)} \\ -\frac{g_2}{g_2+g_3} & \frac{g_2 g_3}{g_2+g_3} \end{bmatrix}$$

I-6



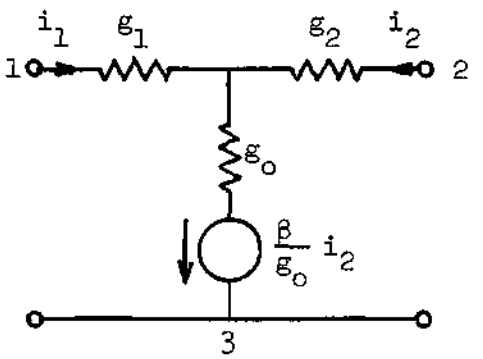
$$\begin{bmatrix} \frac{(\beta+1)g_3+g_2+g_o}{g_o(g_2+g_3)} & \frac{\beta g_2 g_3+g_2 g_o}{g_o(g_2+g_3)} \\ -\frac{g_2}{g_2+g_3} & \frac{g_2 g_3}{g_2+g_3} \end{bmatrix}$$

I-7



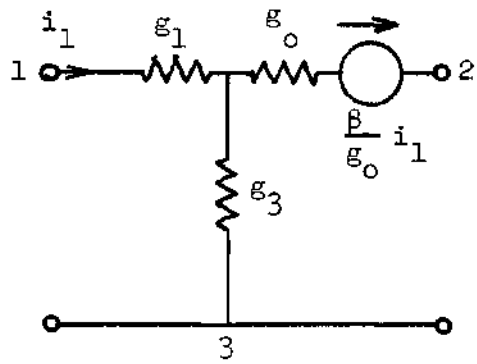
$$\begin{bmatrix} \frac{g_o+g_1+g_2-\beta g_1}{g_1(g_o+g_2)} & \frac{g_2}{g_o+g_2} \\ \frac{(\beta-1)g_2}{g_o+g_2} & \frac{g_o g_2}{g_o+g_2} \end{bmatrix}$$

I-8



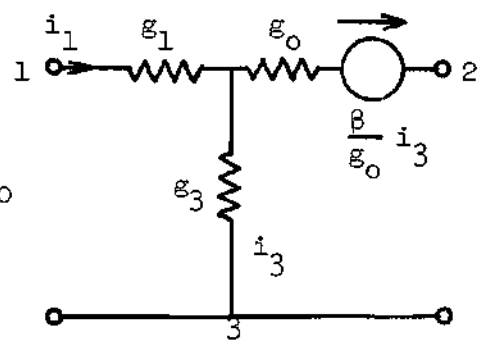
$$\begin{bmatrix} \frac{g_1+(1-\beta)g_2+g_o}{g_1[(1-\beta)g_2+g_o]} & -\frac{(\beta-1)g_2}{(1-\beta)g_2+g_o} \\ -\frac{g_2}{(1-\beta)g_2+g_o} & \frac{g_o g_2}{(1-\beta)g_2+g_o} \end{bmatrix}$$

I-9



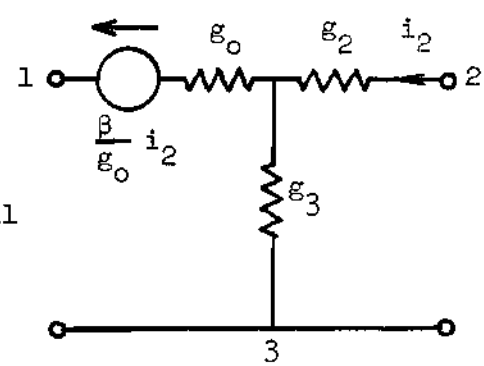
$$\begin{bmatrix} \frac{(1-\beta)g_1+g_3+g_o}{g_1(g_o+g_3)} & \frac{g_o}{g_o+g_3} \\ -\frac{(g_o+\beta g_3)}{g_o+g_3} & \frac{g_o g_3}{g_o+g_3} \end{bmatrix}$$

I-10



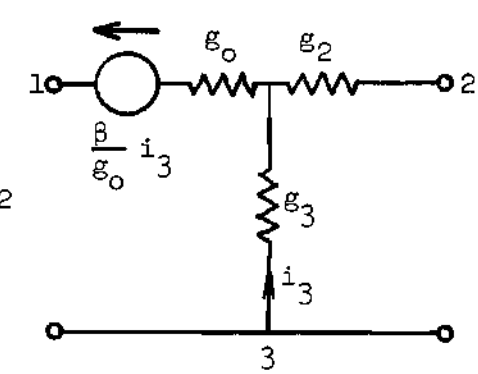
$$\begin{bmatrix} \frac{1}{g_1} + \frac{1}{(g_o+g_3-\beta g_3)} & \frac{g_o}{(1-\beta)g_3+g_o} \\ \frac{\beta g_3-g_o}{(1-\beta)g_3+g_o} & \frac{g_o g_3}{(1-\beta)g_3+g_o} \end{bmatrix}$$

I-11



$$\begin{bmatrix} \frac{(1-\beta)g_2+g_3+g_o}{g_o(g_2+g_3)} & \frac{g_2(g_o+\beta g_3)}{g_o(g_2+g_3)} \\ -\frac{g_2}{g_2+g_3} & \frac{g_2 g_3}{g_2+g_3} \end{bmatrix}$$

I-12



$$\begin{bmatrix} \frac{g_2+(1-\beta)g_3+g_o}{g_o(g_2+g_3)} & \frac{g_2(\beta g_3-g_o)}{g_o(g_2+g_3)} \\ -\frac{g_2}{g_2+g_3} & \frac{g_2 g_3}{g_2+g_3} \end{bmatrix}$$

APPENDIX V

COMPUTER PROGRAM OF THE NIC V5-V12 FREQUENCY RESPONSE

```
          BEGIN

COMMENT         FREQUENCY RESPONSE OF THE NIC V5-V12;
FILE IN         CARDCK (2,10);
FILE OUT        LINECK 6(6,15);
FORMAT          FM1(X7,"F",X20,"R",X25,"X");


FORMAT          FM2(R11.1,X10,R14.4,X10,R14.4);


INTEGER         I;
REAL            X,W,R,F,YL,ZL,NR,NI,DR,DI,GM,CSG,CDG,K;
REAL            A0,A1,A2,A3,B0,B1,B2,B3;
LIST            L1(GM,CDG,CSG,ZL);
LIST            L2(F,R,X);
PROCEDURE       COMP;
          BEGIN
                YL←1/ZL;
                A3←0;
                A2←-CSG*2;
                A1←2×(2×GM×CDG-GM×CSG+YL×CSG);
                A0←GM×(2×YL-GM);
                B3←0;
                B2←YL×CSG*2+2×GM×CDG×CSG;
                B1←2×GM×(YL×CSG+GM×CDG);
                B0←YL×GM*2;
                W←6.28×F;
                NR←A0-A2×W*2;
                NI←A1×W-A3×W*3;
                DR←B0-B2×W*2;
                DI←B1×W-B3×W*3;
                R←(NR×DR+NI×DI)/(DR*2+DI*2);
                X←(NI×DR-DI×NR)/(DR*2+DI*2);
                WRITE (LINECK,FM2,L2);
          END COMP;
                WRITE (LINECK[NO]);
                READ (CARDCK,/,L1);
                CLOSE (CARDCK,RELEASE);
                WRITE (LINECK,FM1);
                FOR I←1 STEP 1 UNTIL 6 DO
```

```
BEGIN
      K←10*I;
      F←K;
      COMP;
      F←2×K;
      COMP;
      F←3×K;
      COMP;
      F←4×K;
      COMP;
      F←5×K;
      COMP;
      F←6×K;
      COMP;
      F←7×K;



      COMP;
      F←8×K;
      COMP;
      F←9×K;
      COMP;
END   ;
END   .
```

F	R	X
10.0	-500.0000	0.0087
20.0	-500.0000	0.0173
30.0	-500.0000	0.0260
40.0	-500.0000	0.0347
50.0	-500.0000	0.0433
60.0	-500.0000	0.0520
70.0	-500.0000	0.0607
80.0	-500.0000	0.0693
90.0	-500.0000	0.0780
100.0	-500.0000	0.0867
200.0	-500.0000	0.1733
300.0	-500.0000	0.2600
400.0	-499.9999	0.3467
500.0	-499.9999	0.4333
600.0	-499.9999	0.5200
700.0	-499.9998	0.6066
800.0	-499.9998	0.6933
900.0	-499.9997	0.7800
1000.0	-499.9996	0.8666
2000.0	-499.9984	1.7333
3000.0	-499.9965	2.5999
4000.0	-499.9938	3.4665
5000.0	-499.9903	4.3332
6000.0	-499.9860	5.1998
7000.0	-499.9810	6.0664
8000.0	-499.9752	6.9330
9000.0	-499.9686	7.7996
10000.0	-499.9612	8.6662
20000.0	-499.8450	17.3315
30000.0	-499.6512	25.9948
40000.0	-499.3800	34.6553
50000.0	-499.0314	43.3118
60000.0	-498.6055	51.9635
70000.0	-498.1024	60.6094
80000.0	-497.5221	69.2485
90000.0	-496.8648	77.8799
100000.0	-496.1307	86.5024
200000.0	-484.6026	172.0431
300000.0	-465.6510	255.6920
400000.0	-439.6550	336.5828
500000.0	-407.1192	413.9377
600000.0	-368.6499	487.0878
700000.0	-324.9291	555.4869
800000.0	-276.6865	618.7175
900000.0	-224.6731	676.4912
1000000.0	-169.6368	728.6426
2000000.0	414.3721	966.7908
3000000.0	854.8779	886.6865
4000000.0	1122.0324	710.4044
5000000.0	1274.9373	525.6609
6000000.0	1359.1394	356.5127

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